BSI Technology with Bulk Si Wafer

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June 25 2009

Acknowledgement

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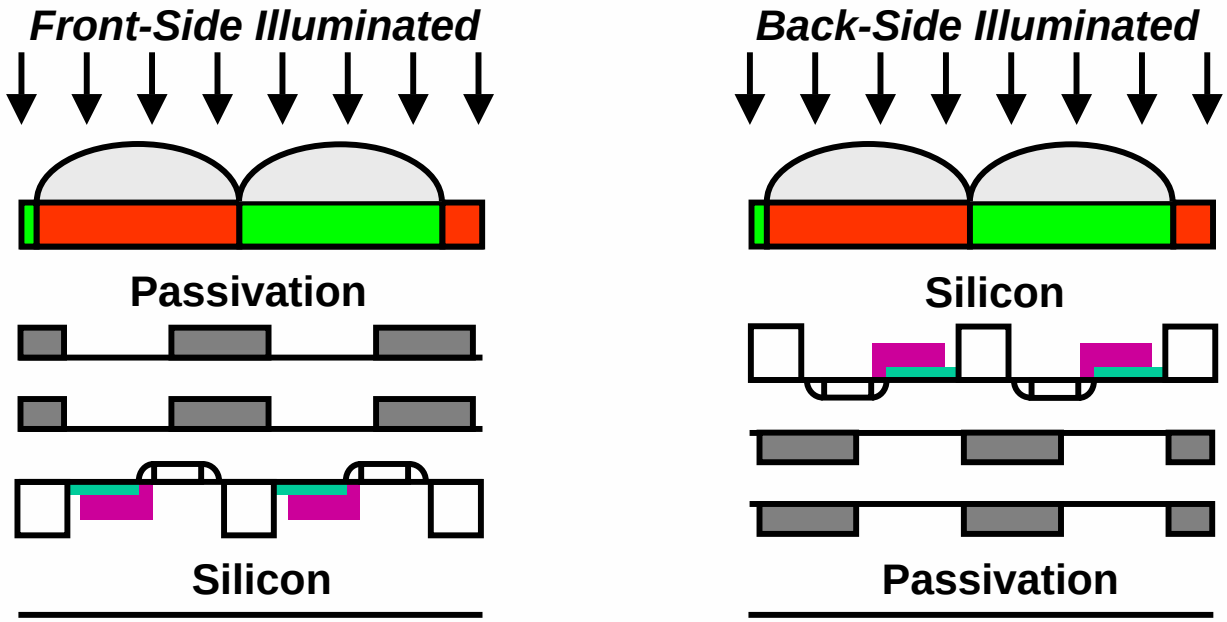
Outline

- Overview
- Si Technology
- Color filter & Microlens
- Manufacturability
- Device Performance
- BSI Package
- Summary & Future Trend
- Reference

BSI Overview

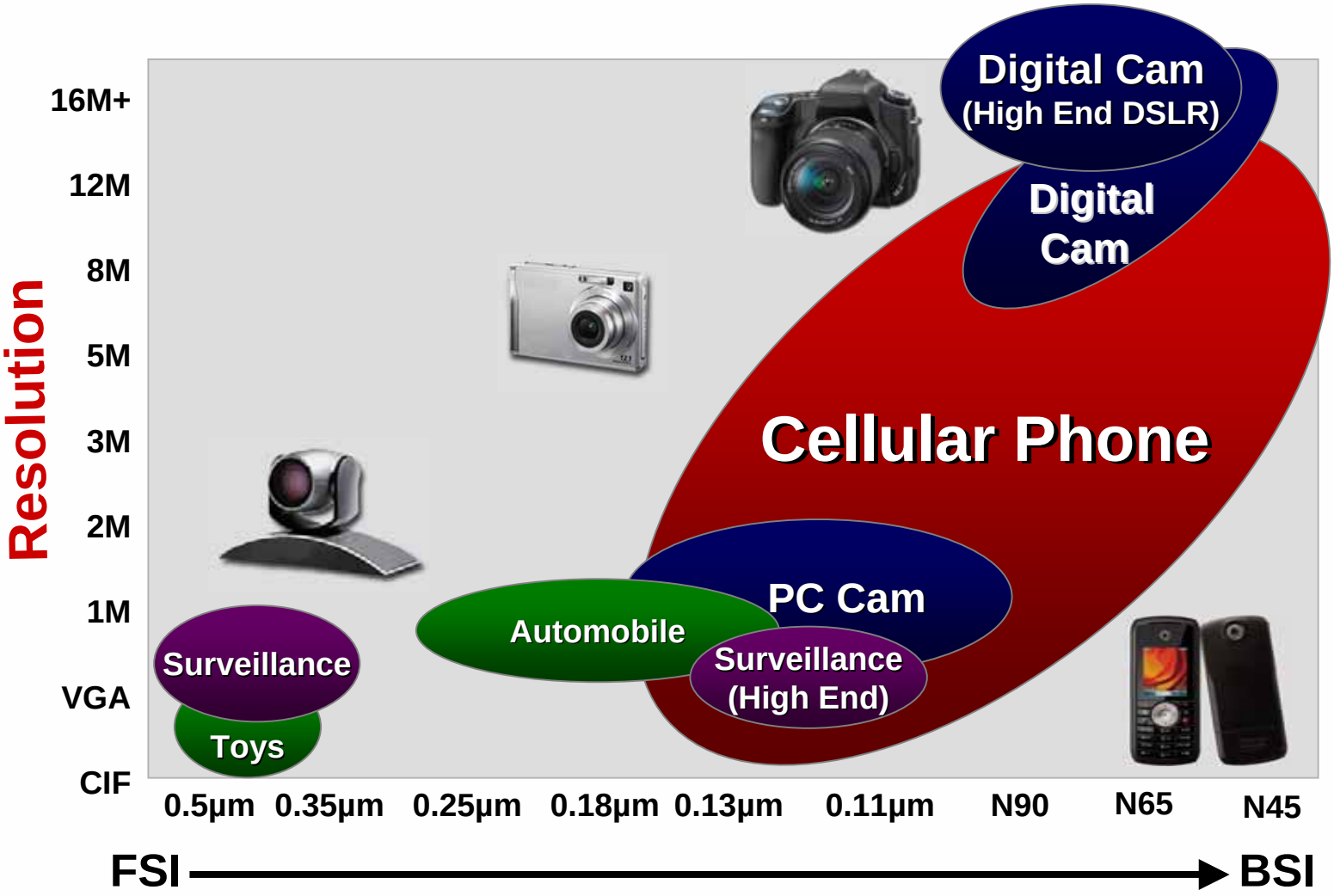
What's BSI

- **Back-Side Illuminated CIS**



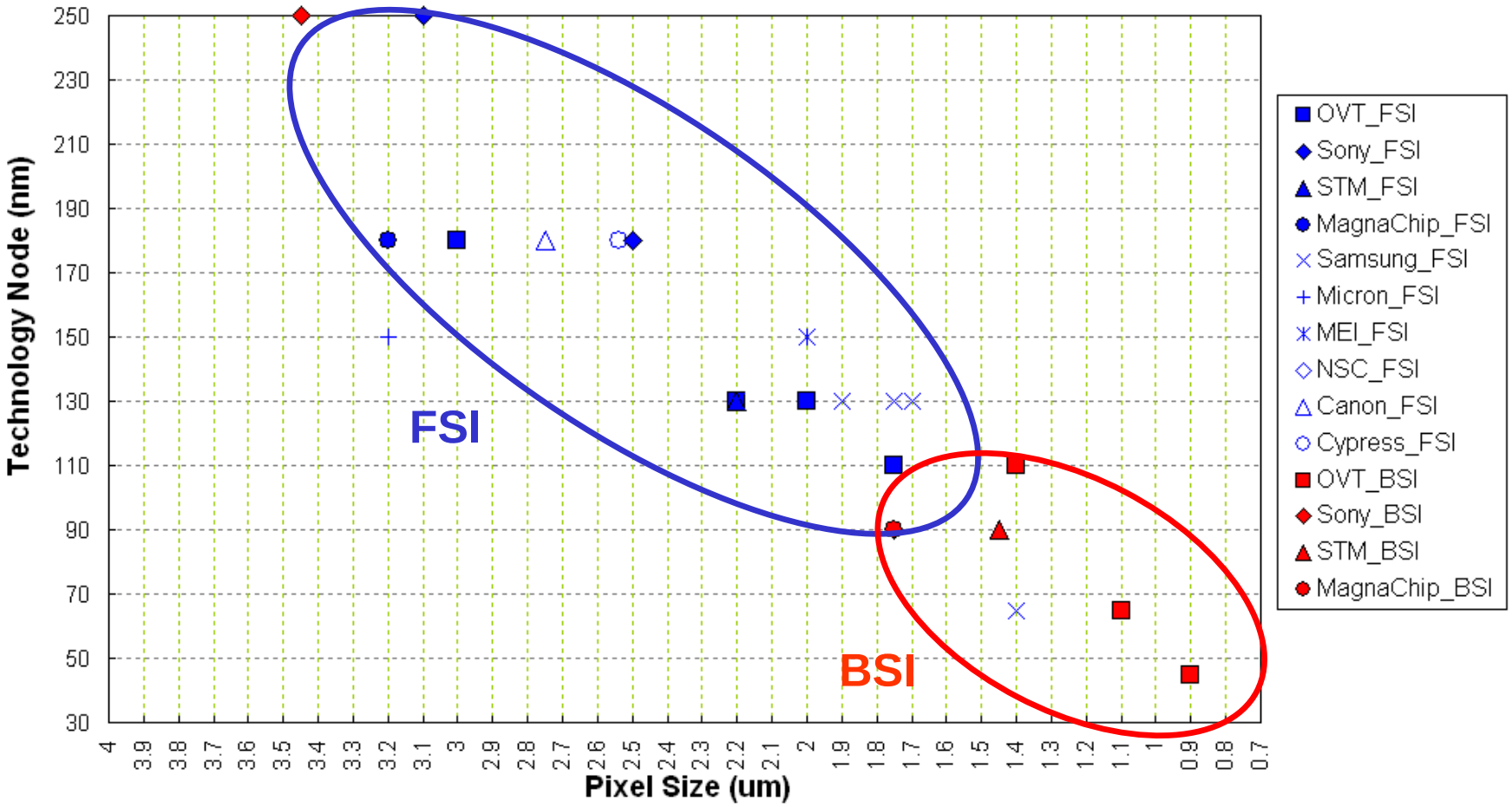
- **Short optical path: better sensitivity & crosstalk.**
- **Freedom for metal routing: integration for SOC.**
- **Complex process**

CMOS Sensor Application & Technology



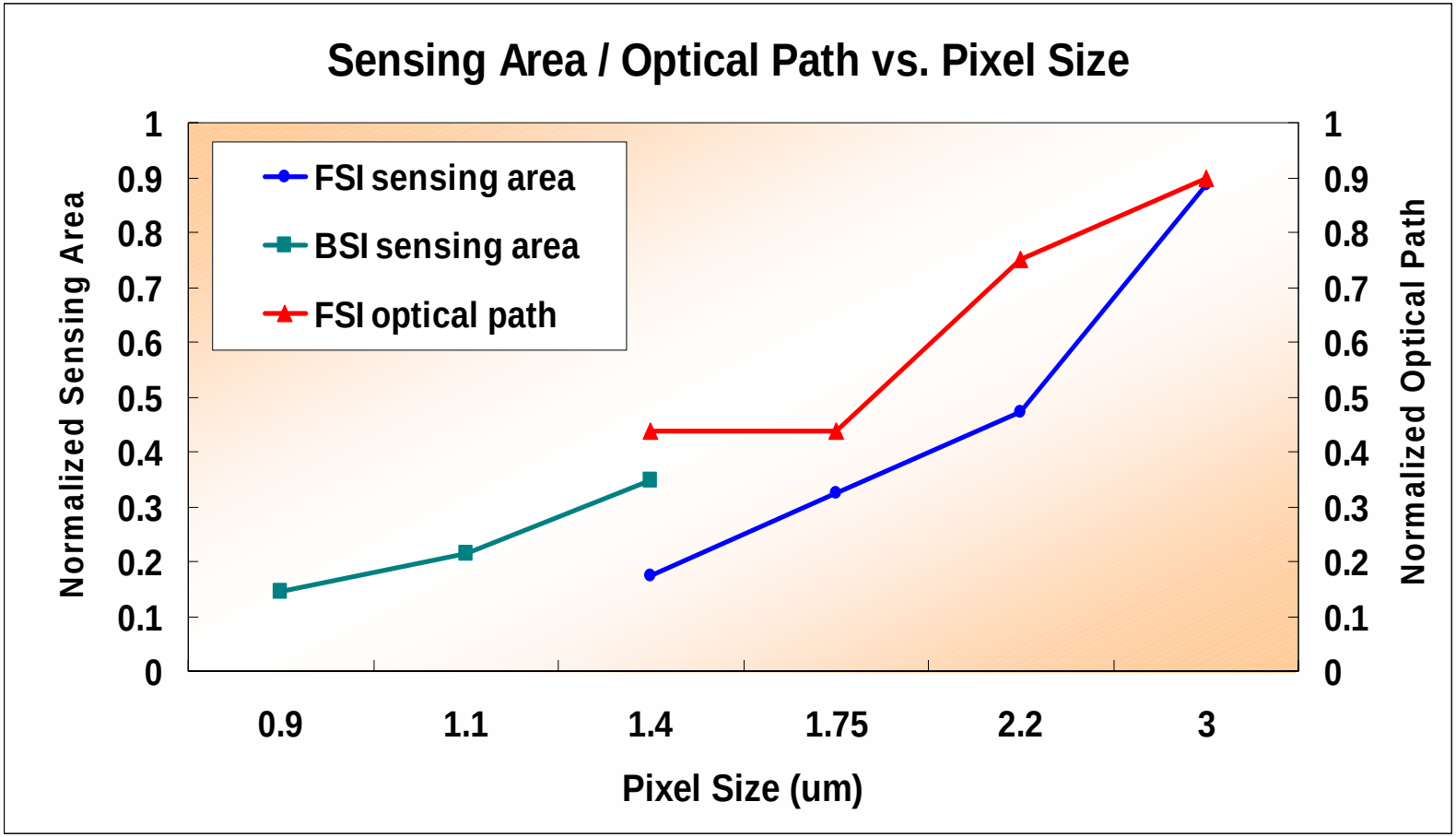
¼" Camera Module	2MP	3MP	5MP	8MP	12MP
Pixel Size	2.2um	1.75um	1.4um	1.1um	0.9um

Scaling Trend of CIS Pixel Size



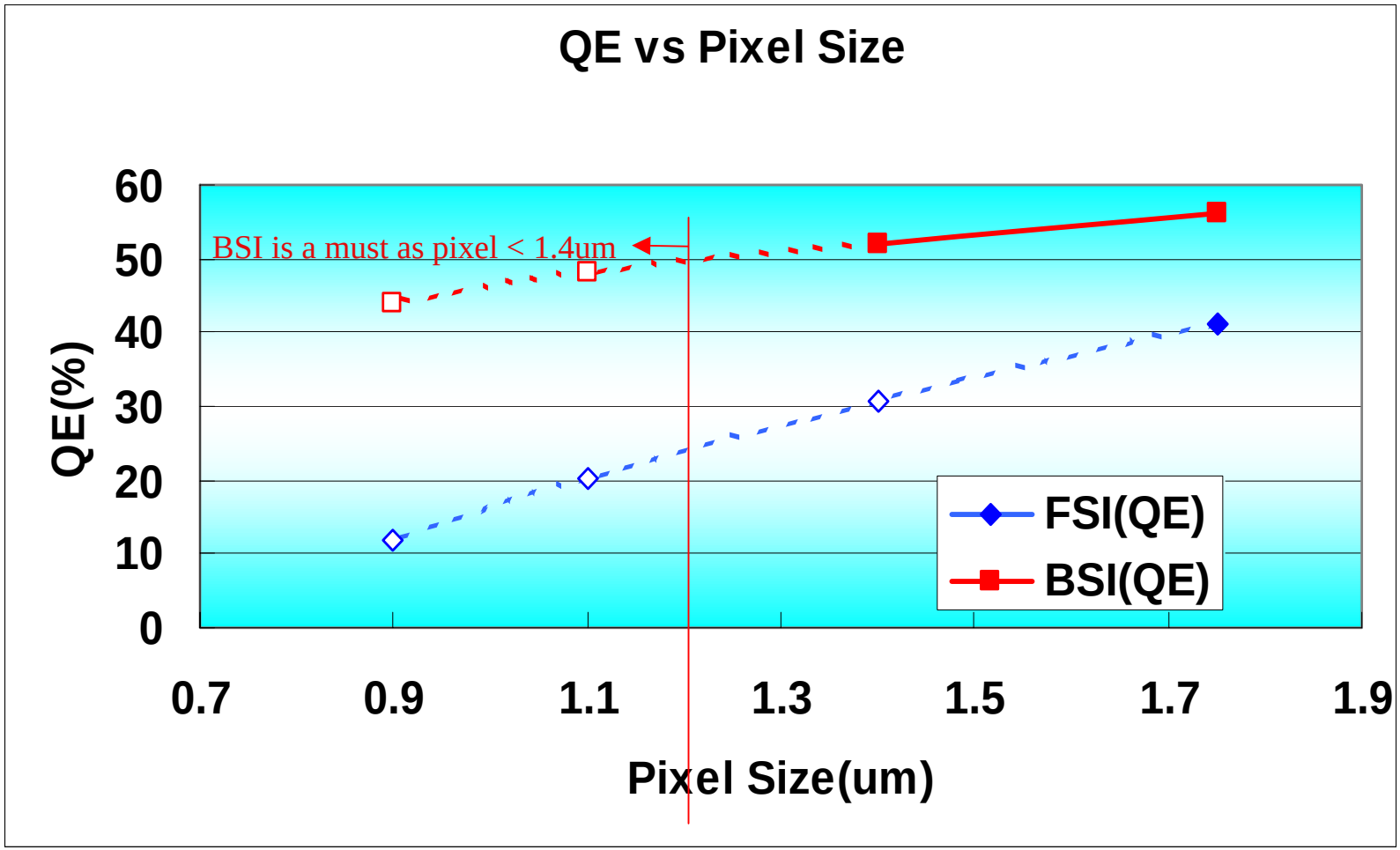
- **Pixel size shrink drives CIS technology node. FSI will transfer to BSI for smaller pixel (< 1.4um) and high performance sensor.**

FSI/BSI Structure Comparison



- Sensing area at 1.4um node: BSI gets double sensing area compare to FSI.
- Optical path: BSI get short optical path. FSI need to thin-down backend THK and saturate to 1.75um.

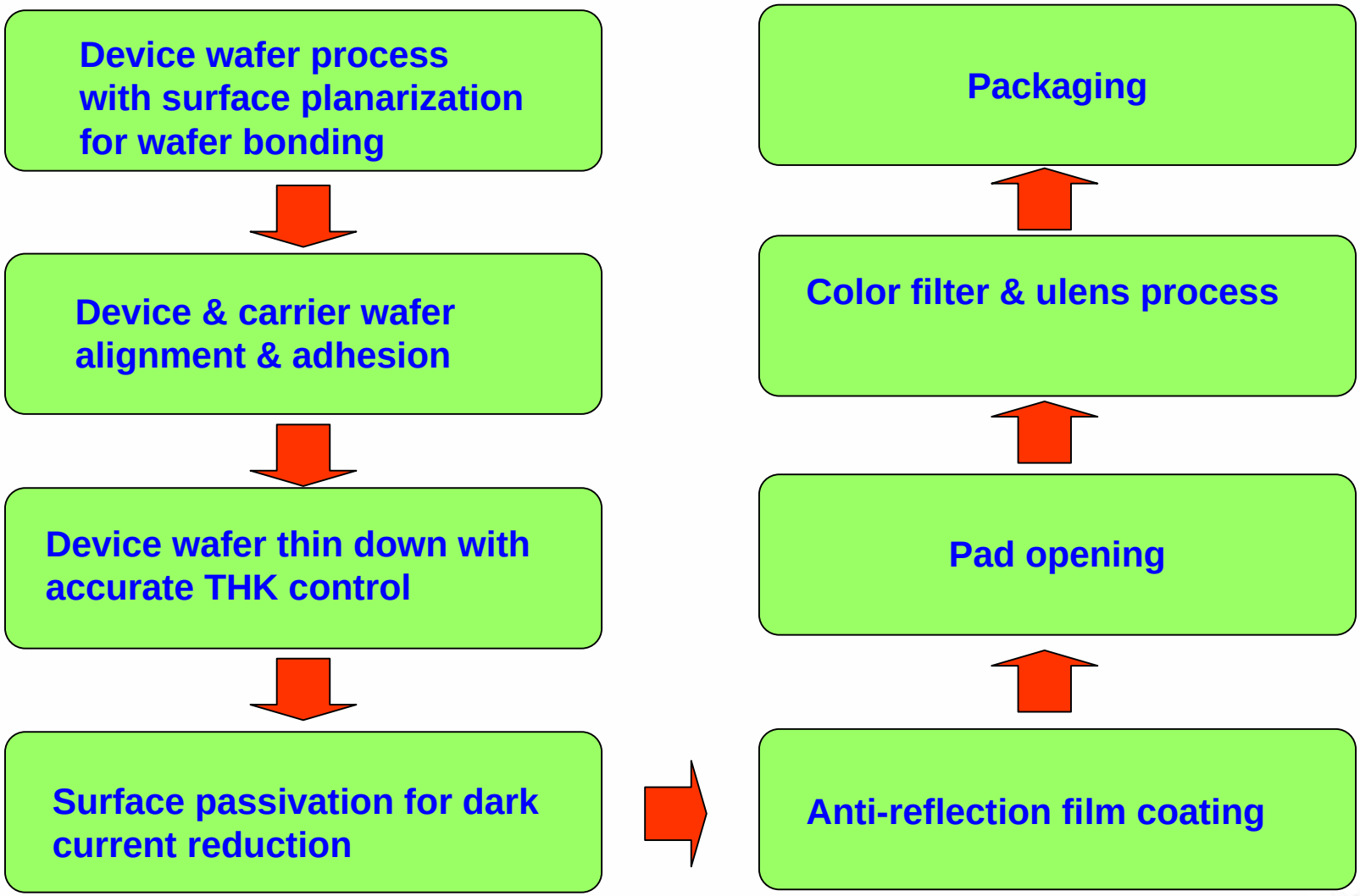
QE Trend Chart (FSI/BSI vs Pixel Size)



- BSI shows higher QE than FSI, especially for smaller pixel size. BSI is “must-use” as pixel < 1.4um to keep an acceptable QE.

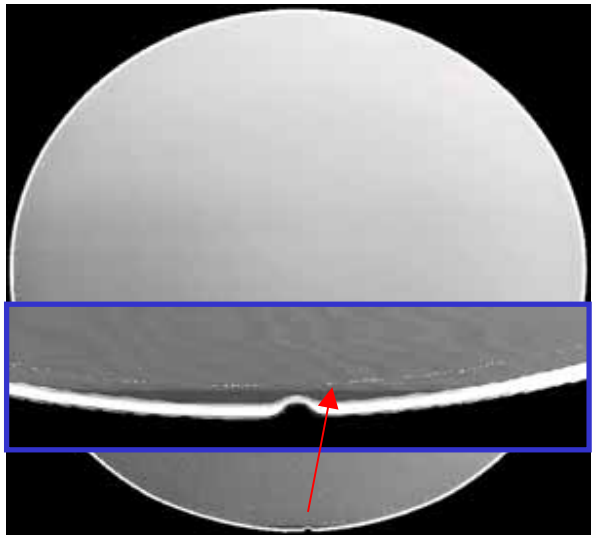
Si Technology in Module & Integration

Schematic of Si Process Flow

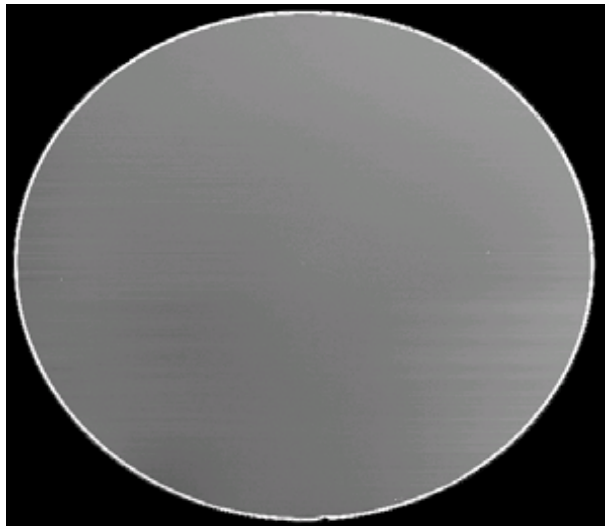


BSI Bonding Progress

- Bubble free achieved
- Bubble monitor methodology established
- Good planarization before bond
- Particle reduction @ bonding interface
- Wafer bonder optimization



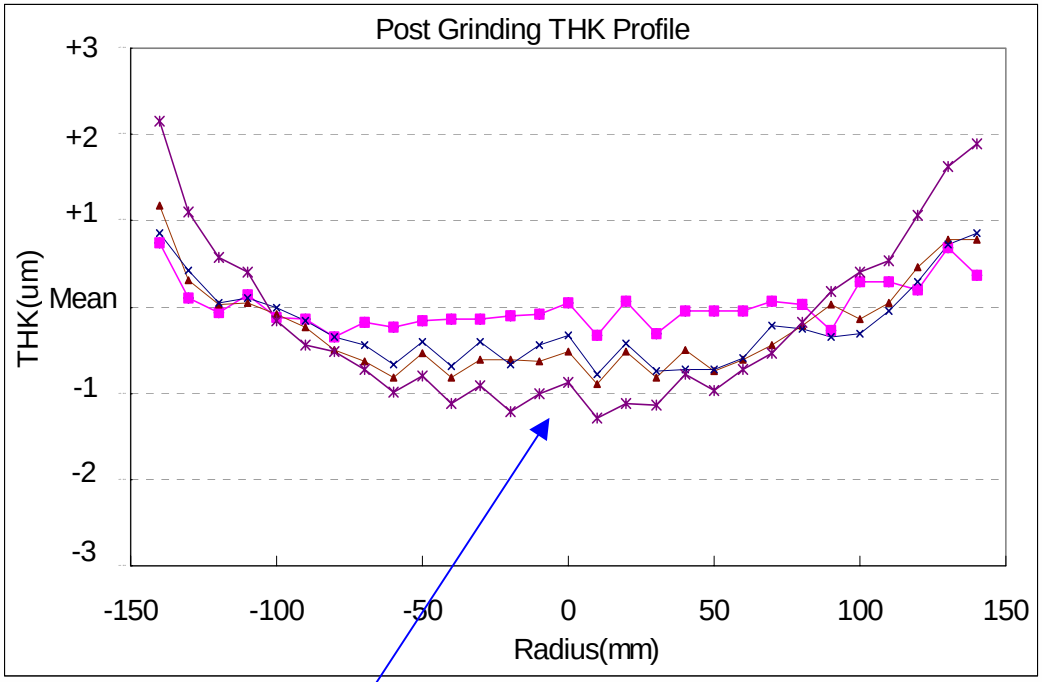
Bubble



Bubble-free

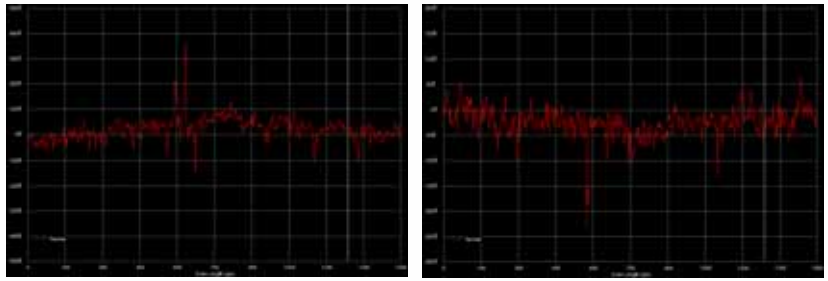
Grinding Performance

- TTW (Total Thickness Variation) within Wafer: 2~3 um
- No visible stripe pattern viewed by OM as demonstrated from small step height < 0.025um within 1.5mm scan range from Alpha-stepper

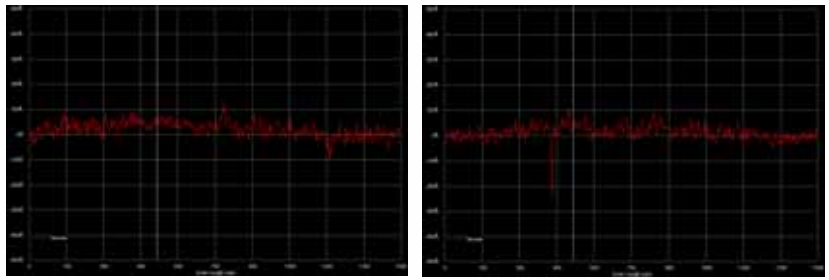


Grinder artificial profile compensation for wet etch thin down process

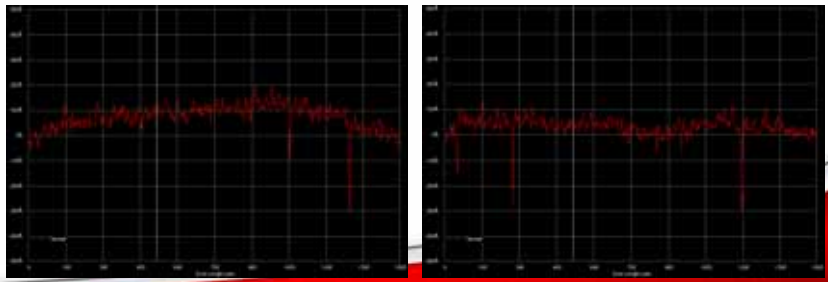
Wafer Center step height ~250A



Wafer Middle step height ~200A

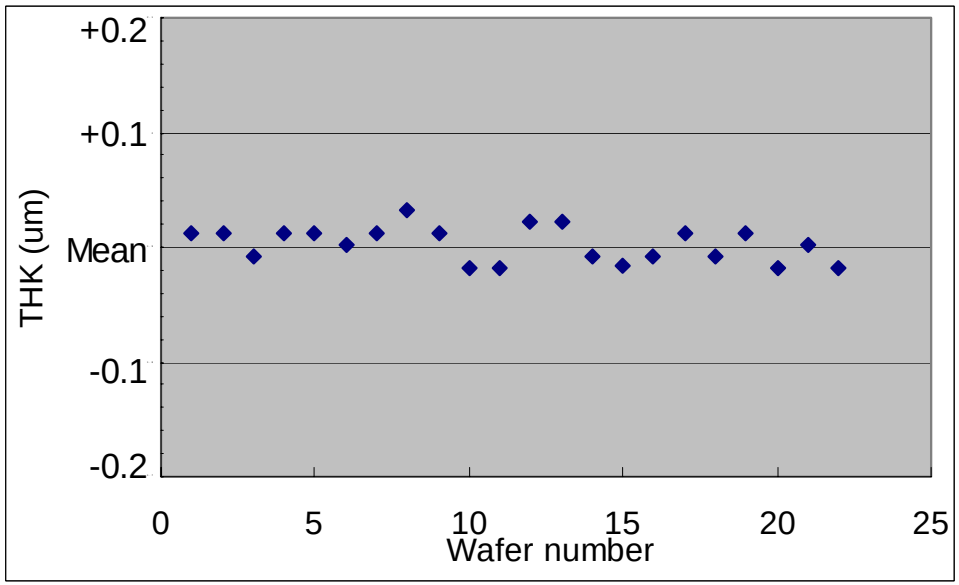


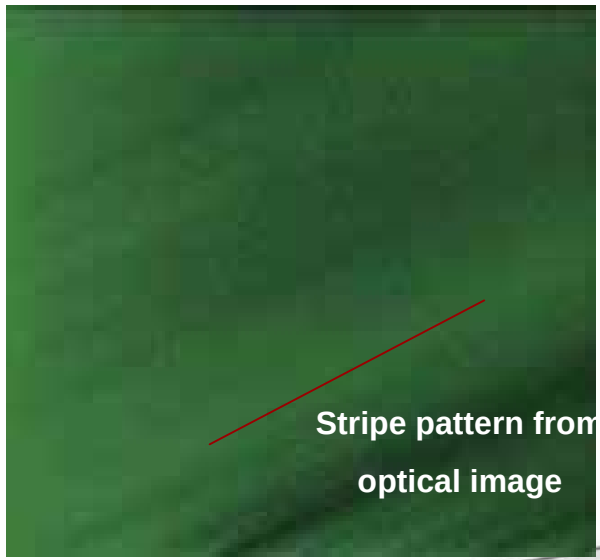
Wafer Edge step height ~230A



BSI Thin Down Process

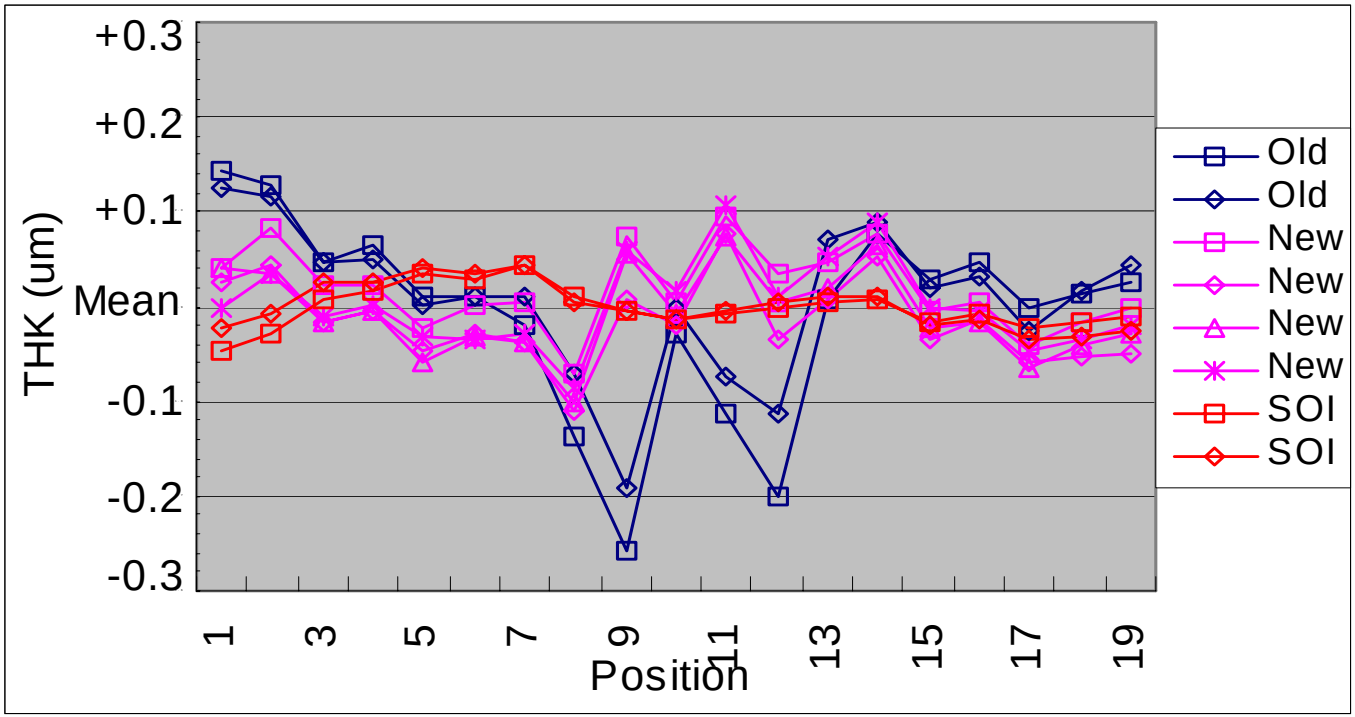
- **Non-SOI approach (TSMC IP chemicals for etch stop on Epi layer)**
- **Mechanical & Wet chemical thin down**
- **WTW THK uniformity controlled @ ≤ +/- 0.025um by establishing feed-forward system**
- **Good surface roughness with stripe pattern free**





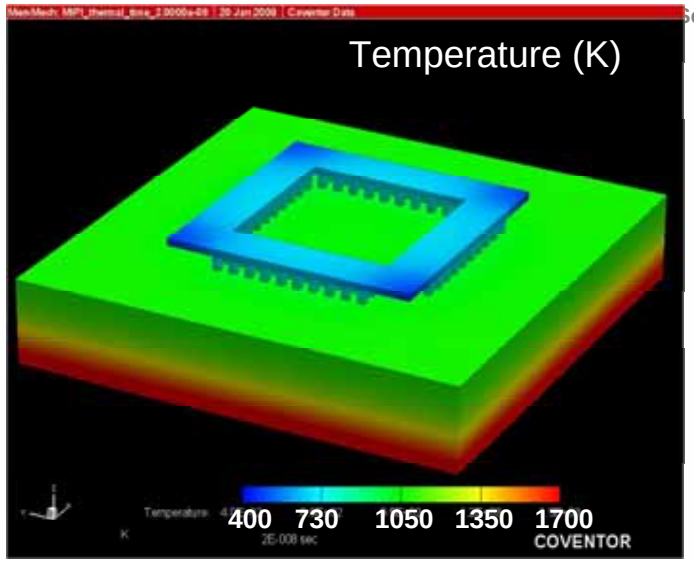
Within Wafer Thickness Uniformity

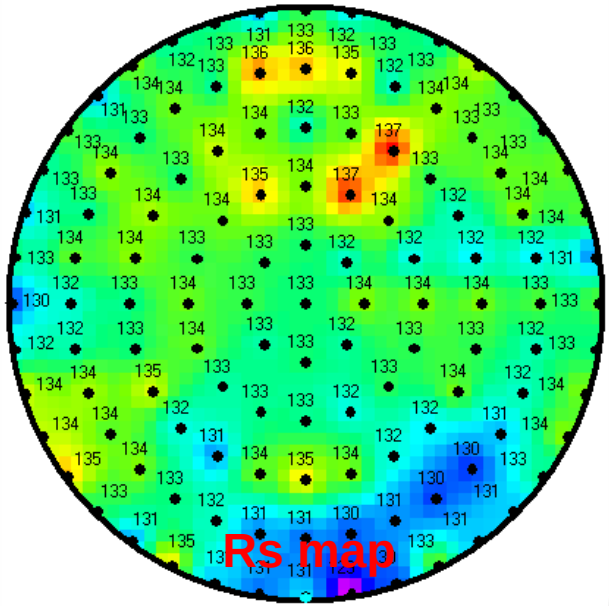
- TTV (Total Thickness Variation) within Wafer < +/- 0.1um
- Epi wafer requires special thin-down technique to maintain reasonable THK variation across wafer
- Si THK variation causes optical response variation

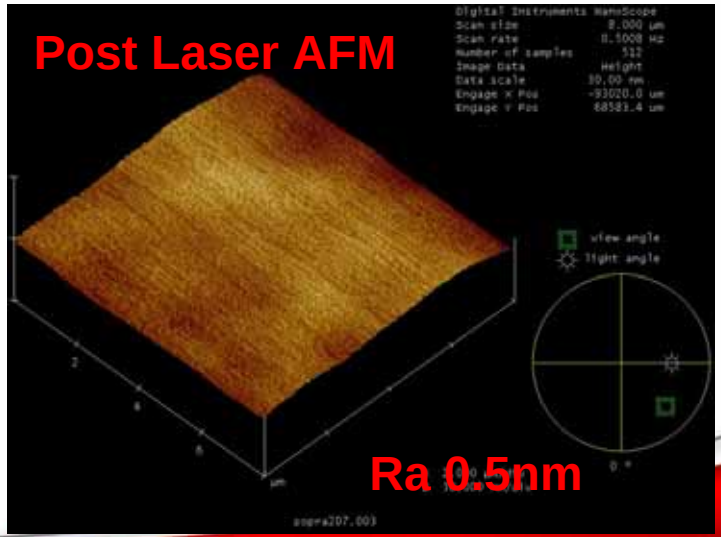


BSI Laser Anneal

- Short wavelength & duration time
- Si melting needed to achieve low Rs (i.e. good activation)
- Good WIW Rs uniformity: ≤ 1.5%
- No thermal damage to device & metal if Si melting
- Good surface roughness

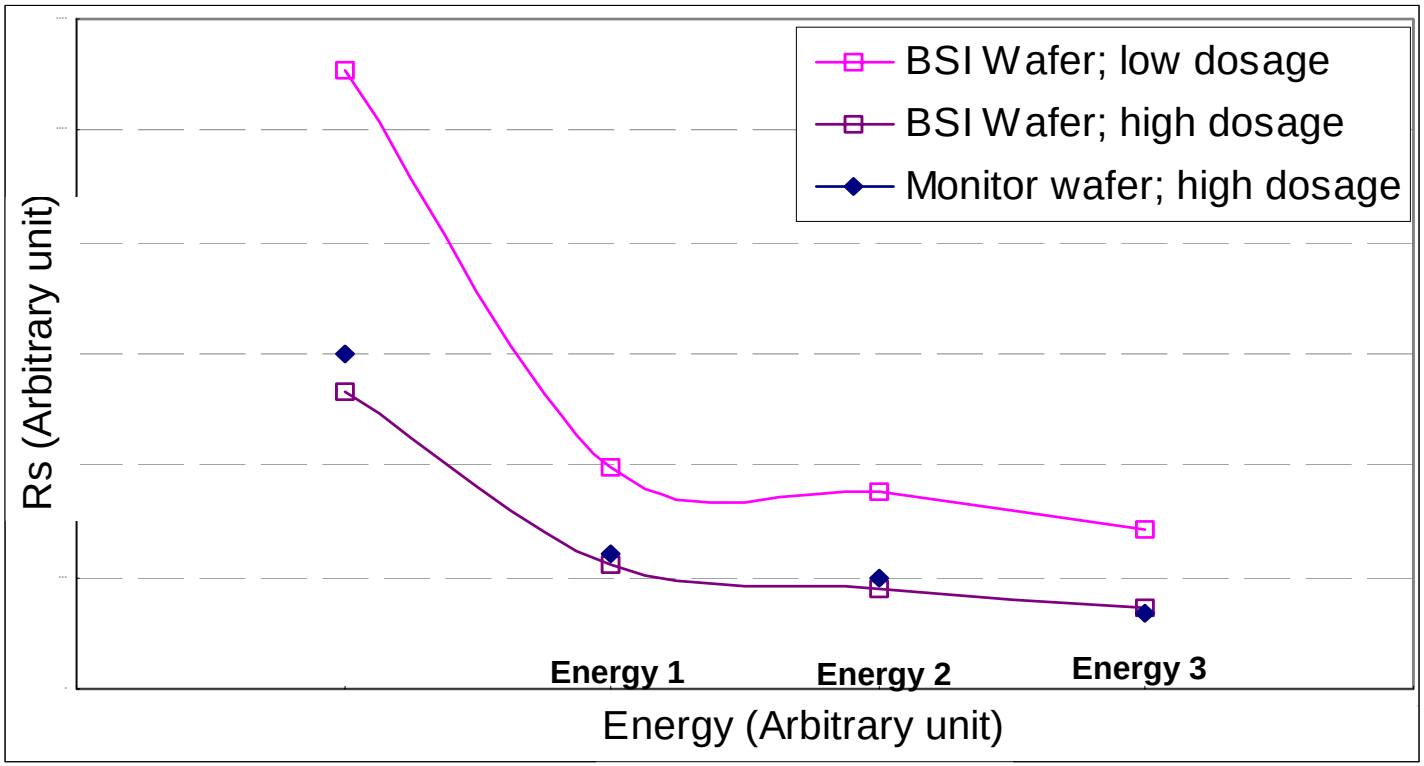






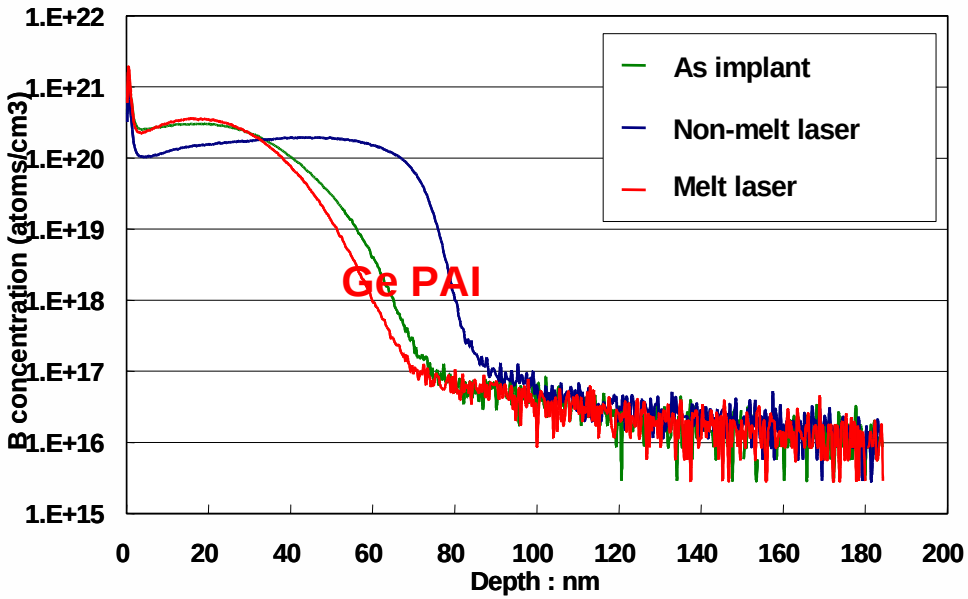
Laser Anneal Rs

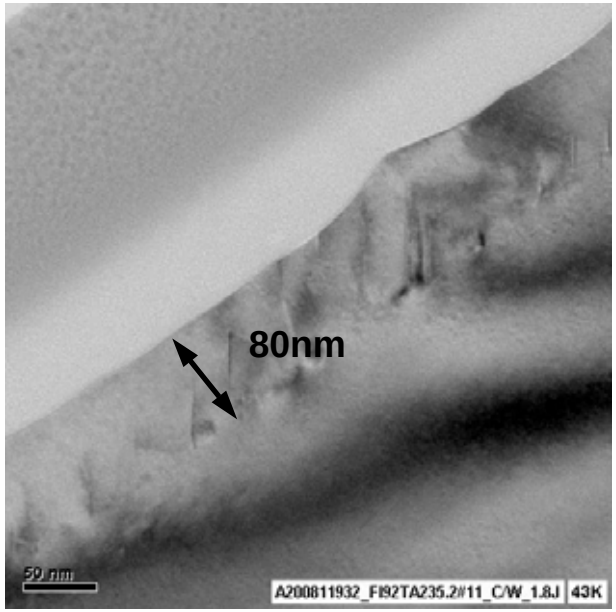
- **BSI Laser Rs verifiaction:**
  - Rs saturates @ Laser energy 1 with Si melting for both high & lo dosage
  - C/W and BSI structure wafers with similar Rs trend



BSI PAI IMP & Crystal Defect

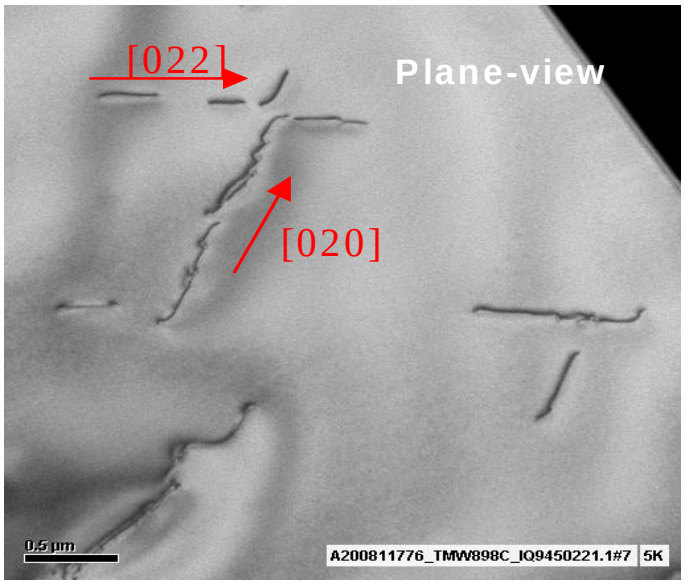
- **PAI implant:**
  - **(111) dislocation found if with melting laser; Defect layer THK matches with SIMS profile**



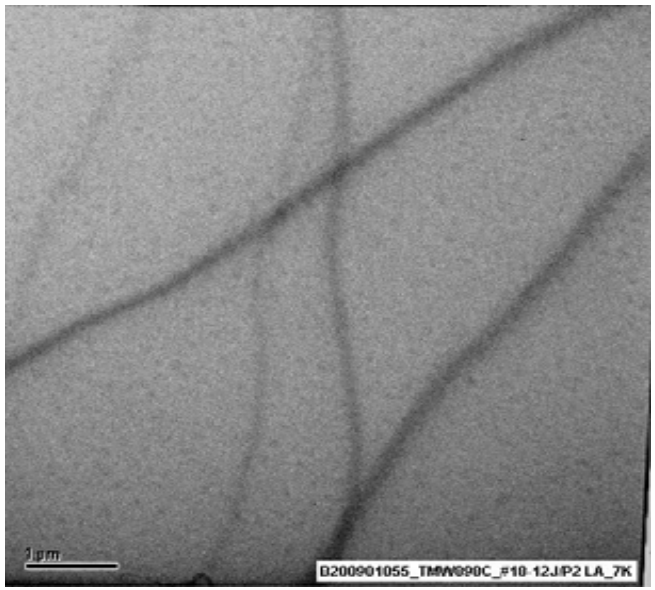


Si TEM for BSI Process Improvement

- **(020)/(022) Crystal defects**
  - **Induced by thin down damage & Si melting/crystallization**
  - **Solved by extra thermal to remove thin down damage before laser anneal**
- **TEM photos show original BSI process with specific defect density and defect free condition for improved process**



Defect density ~0.567/um



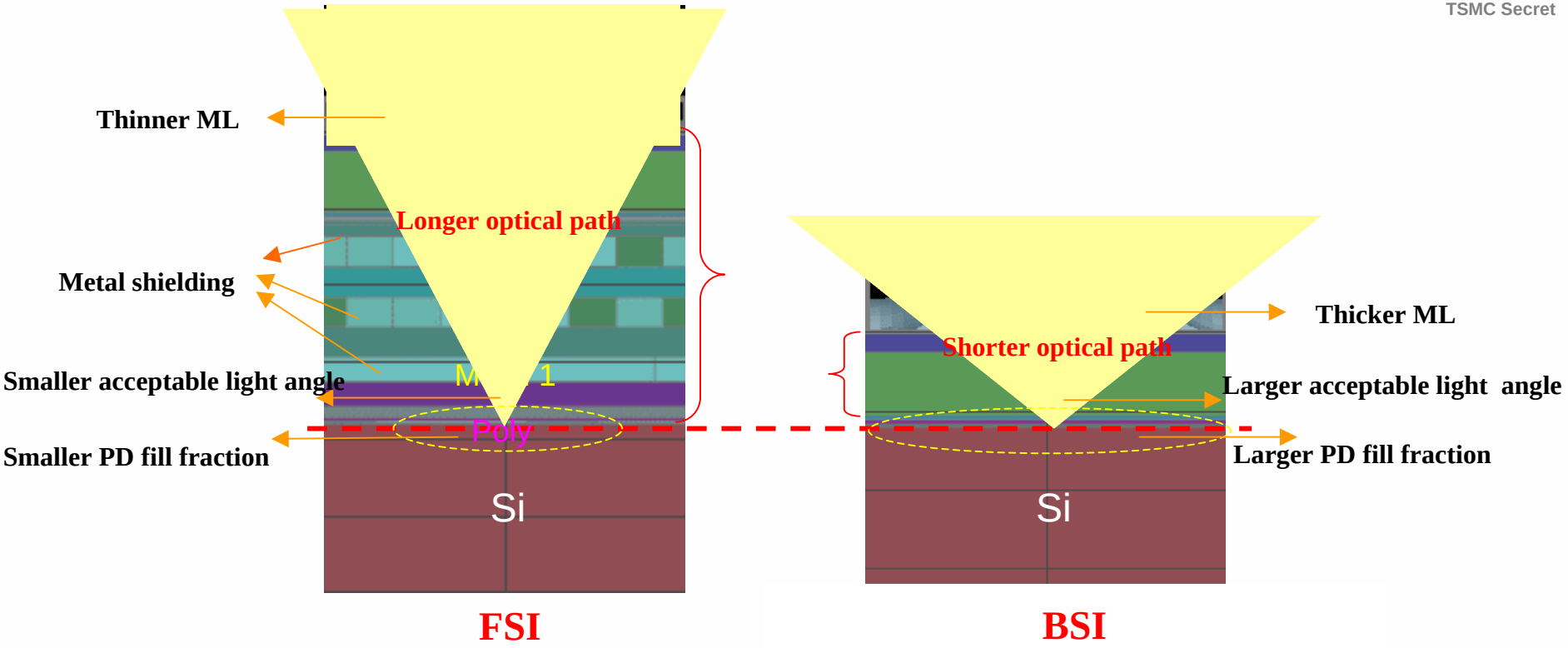
Defect free

BSI Si Technology

- A cost effective thin down approach by using bulk Si wafers with tight Si THK control by feed forward system
- The robust wafer edge integrity achieved by introducing an edge trimming tool
- A bonding recipe & setting with bubble free
- Successfully introduce laser anneal for backside implant activation and crystal defect elimination
- Implementation of backside metal shield for black level reference
- Smooth backside Si surface achieved to minimize its impact to image quality (e.g. stripe pattern, etc.)

Color Filter & Microlens Technology

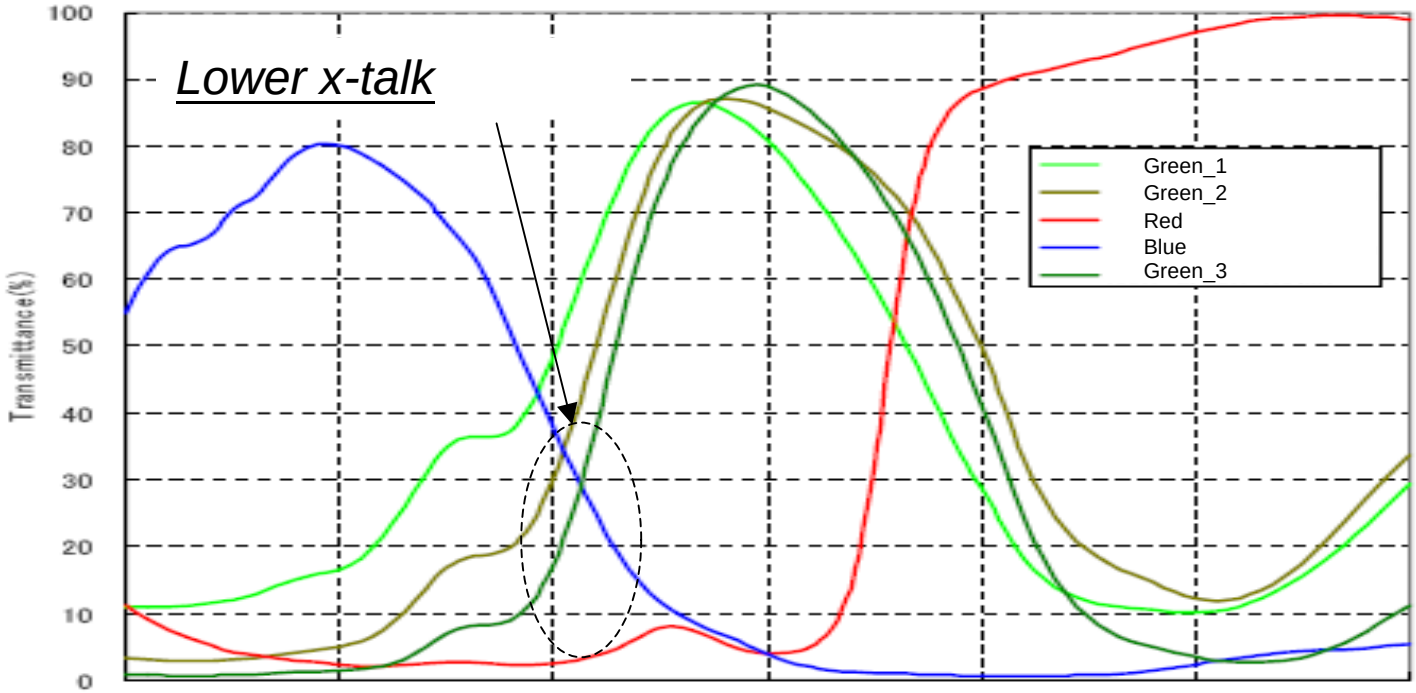
BSI vs FSI Optical Performance



Optical Performance Comparison						
	Optical path	**ML thickness**	**Metal shielding**	**Acceptable light angle**	**PD fill fraction**	**Energy on PD**
FSI	*long*	*thinner*	*yes*	*small (F# 2.8)*	*small (~30%)*	*27%*
BSI	*short*	*thicker*	*no*	*large (F# 2)*	*lager (~50%)*	*56%*

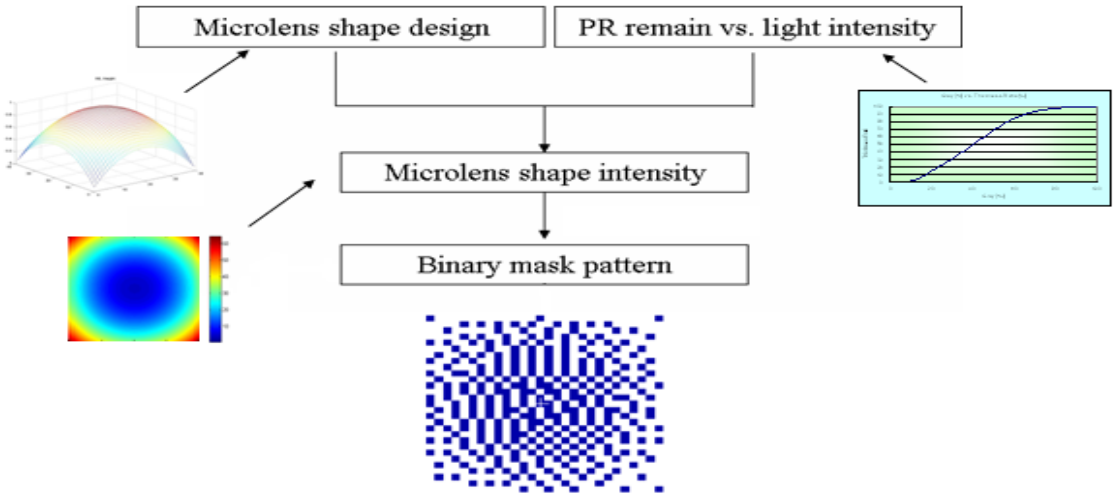
Color Filter in BSI

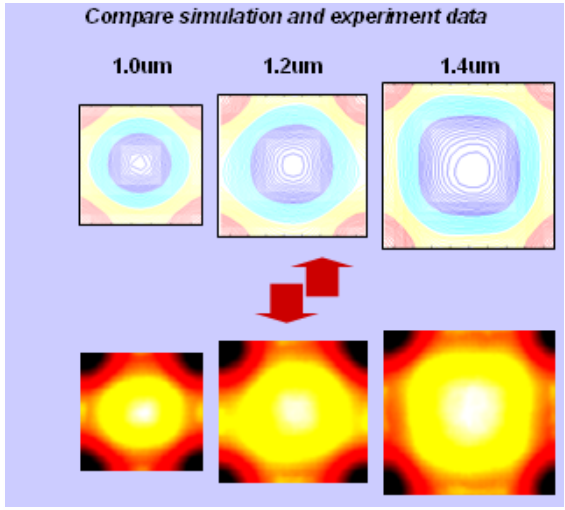
- Variant green color filter material can optimize sensitivity and color X-talk.
  - Green main peak shifts to 550 nm
  - Lower x-talk at green/blue
  - Higher x-talk at green/red



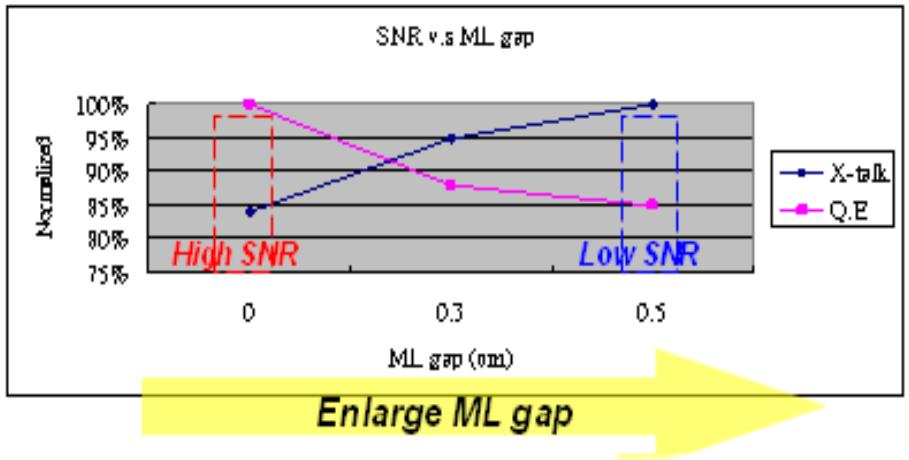
Microlens (ML) Design in BSI

- Grey mask design to enable ML w/ high focusing capability





- **Minimizing ML gap for sensitivity improvement and x-talk reduction**



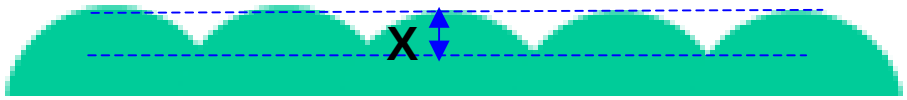
Zero ML gap

ML gap = 0.3 um

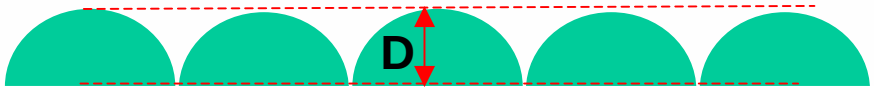
ML gap = 0.5 um

Microlens (ML) Design in BSI

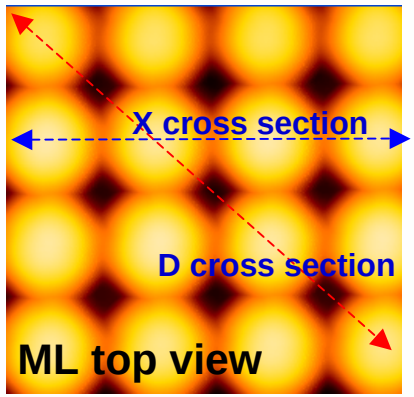
- Grey mask design to enable ML w/ high focusing capability
  - **Control ML height in X,Y(X) and diagonal direction (D) for ML focusing capability**
    - X/D ratio defined as [ML height in x cross section] / [ML height in diagonal cross section] ; For square pixel , ML height in x cross section is equal to ML height in y

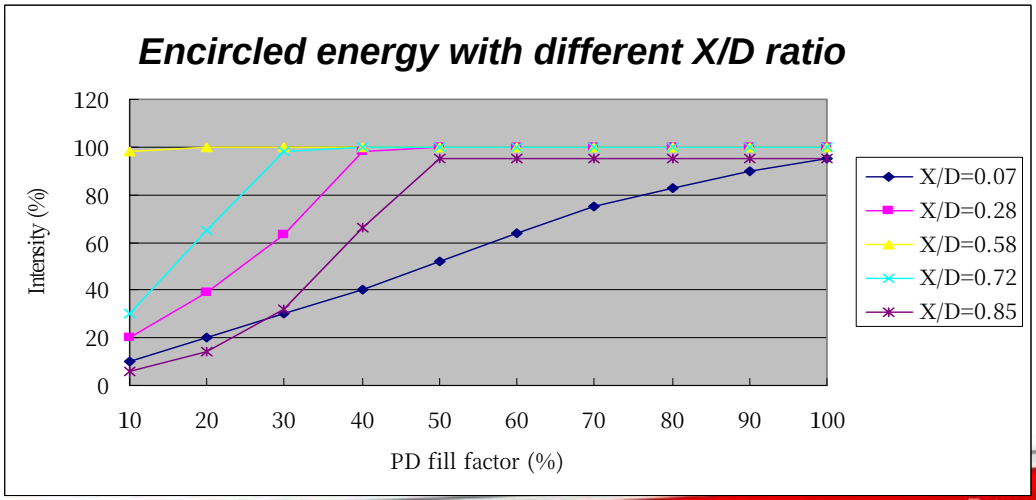


ML profile at x / y cross section



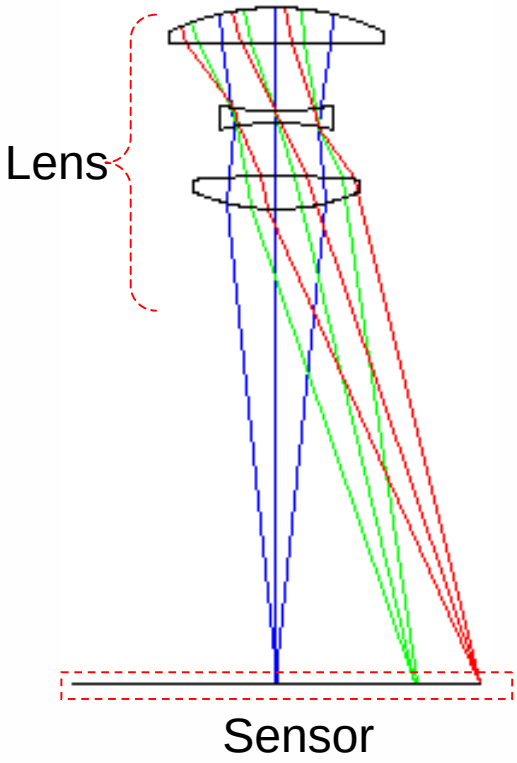
ML height at diagonal cross section

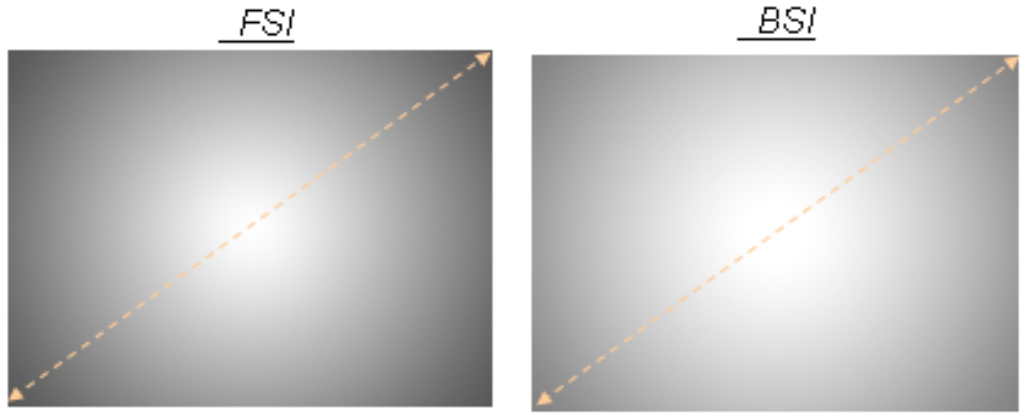


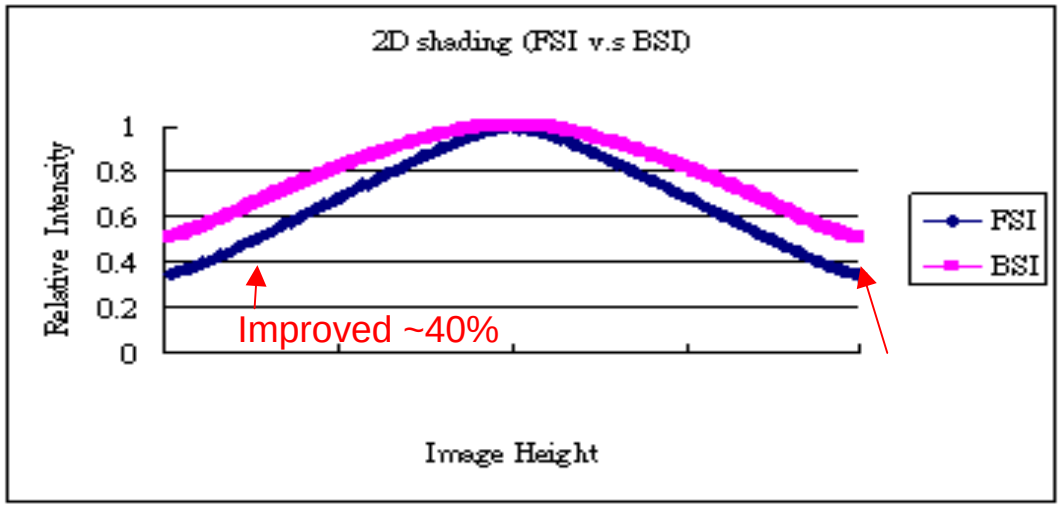


Shading Effect Improvement in BSI

- Compared to FSI, the shading effect in BSI can be improved 40% by integrating sensor and lens in 1.4um pixel

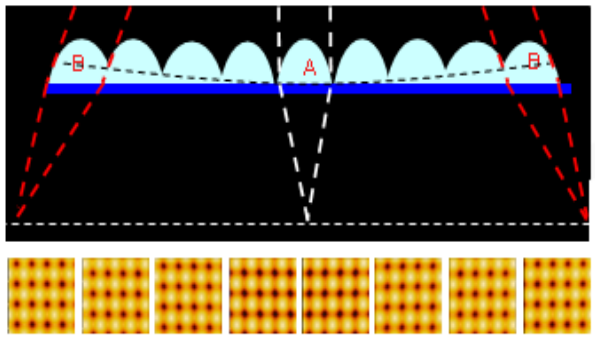


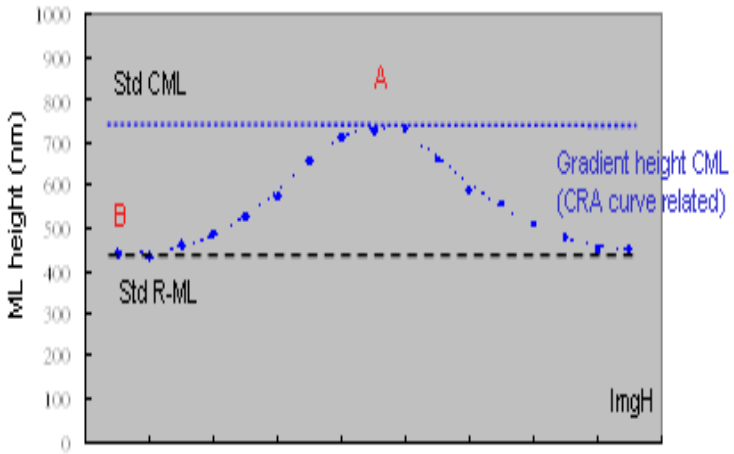


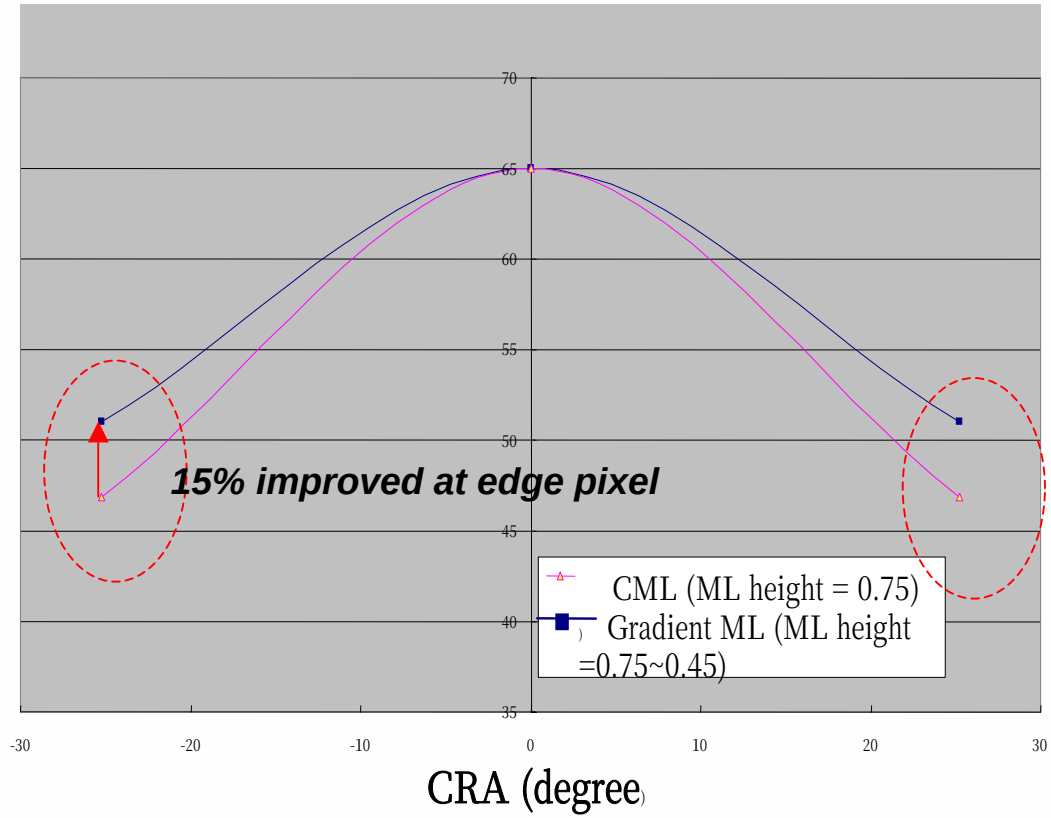


Future Trend-Gradient CML

- Different ML height and shifting arrangement based on CRA
  - **Combined ML shifting and gradient height ML for shading optimization**



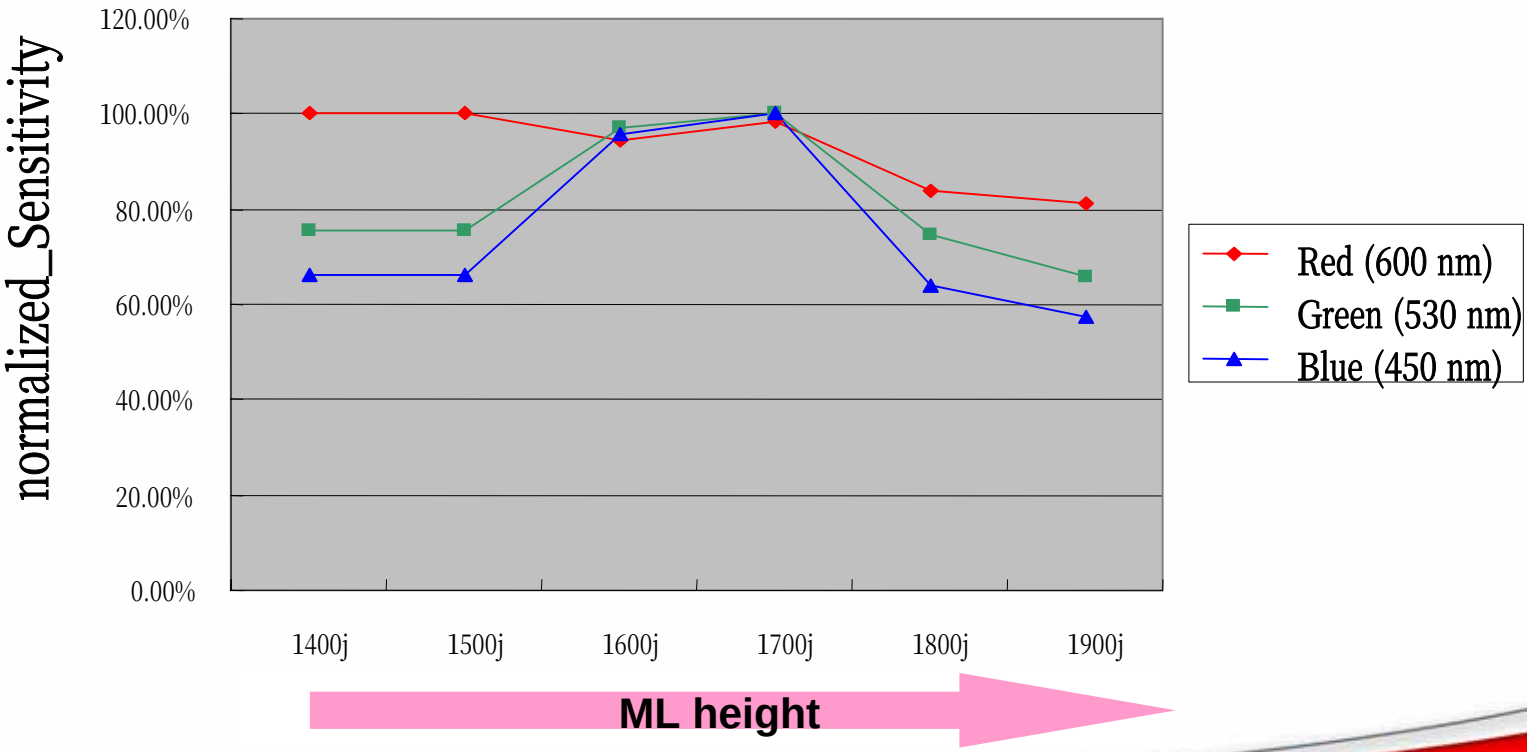




Sensitivity of edge pixel with large CRA
(Shading Profile Simulation)

Future Trend- Optimized ML Height for R/G/B Pixel

- By measurement, the optimized ML height for high sensitivity is different with R/G/B pixels
  - **Thinner ML height with Red pixel and thicker with Green/Blue pixel**



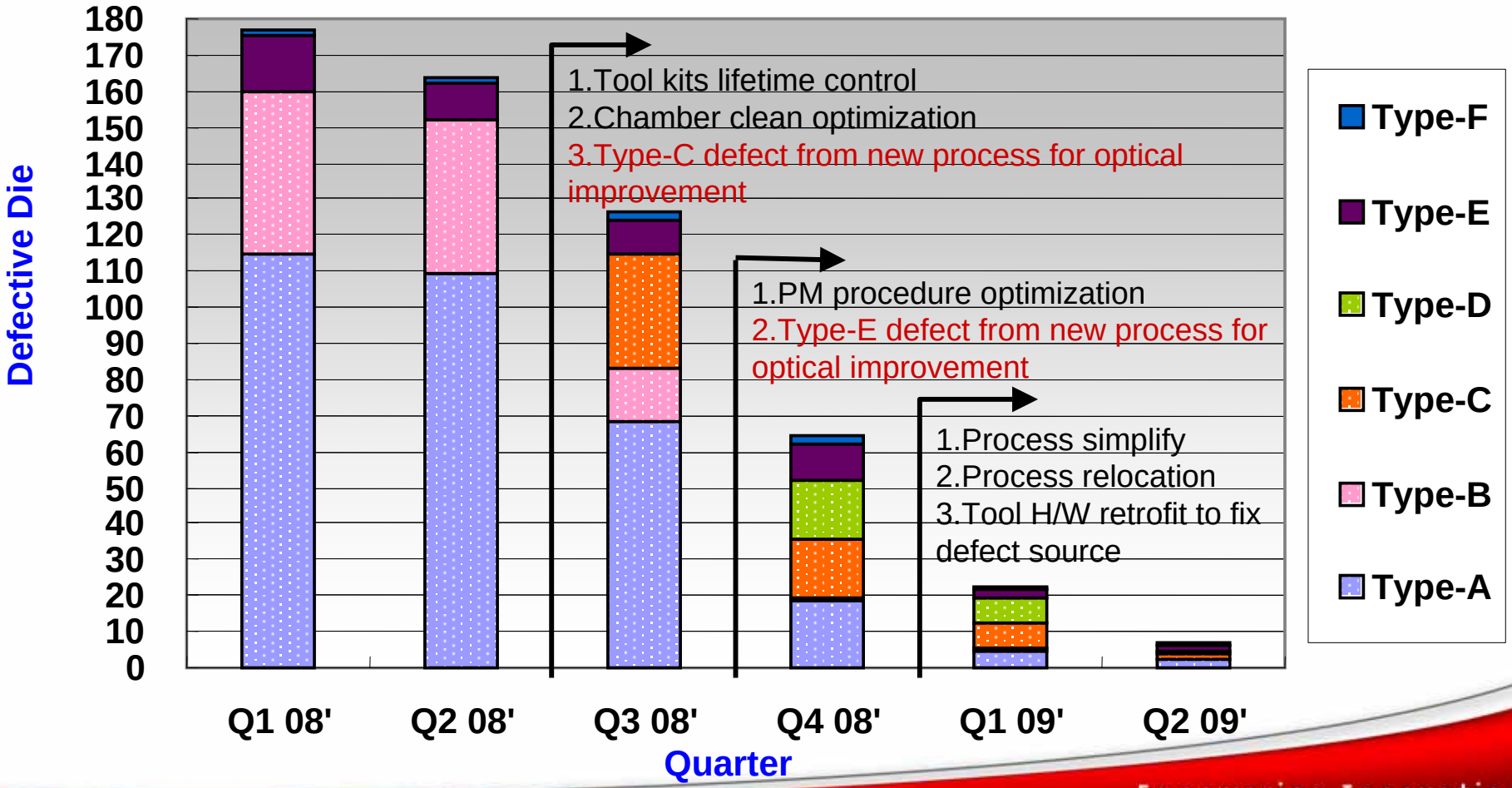
Color Filter/Microlens Development in BSI

- Continuous ML realized on BSI
  - Minimized gap for Q.E improvement and x-talk reduction
  - Shape design
    - Control ML remain thickness on x/y and diagonal for ML focusing capability
- Sensitivity improvement and color X-talk reduction by optimizing color filter material
  - Peak of green shifted to 550 nm
  - Lower x-talk on green-to-blue side
- Gradient CML application
  - Shading performance could be significantly improved in 1.1 um and beyond
    - Optimized ML height by pixels (based on lens' CRA)
- ML profile optimization based on R/G/B pixels
  - To achieve best Q.E and x-talk performance for R/G/B pixels respectively

BSI Manufacturability

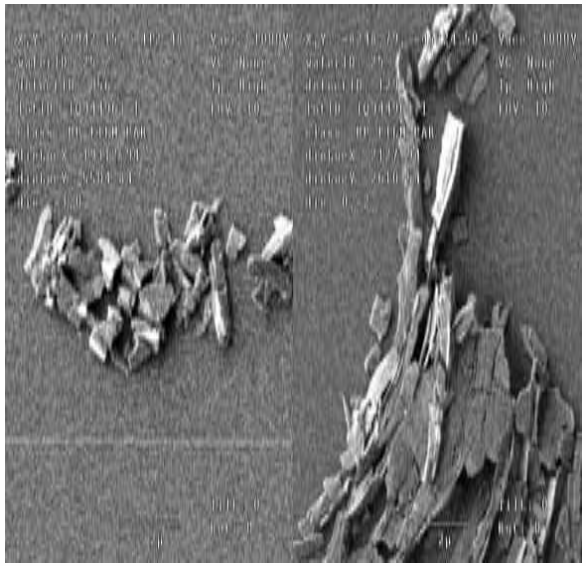
BSI Inline Defect Readiness

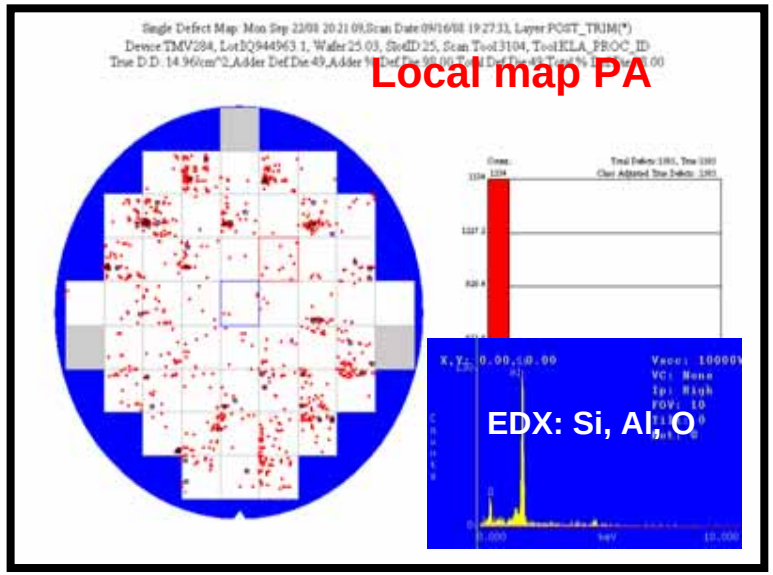
- Major defect sources from wafer thin down, wafer edge integrity, film peeling
- Target for total defective dies: 10



Trimmer Particle Reduction

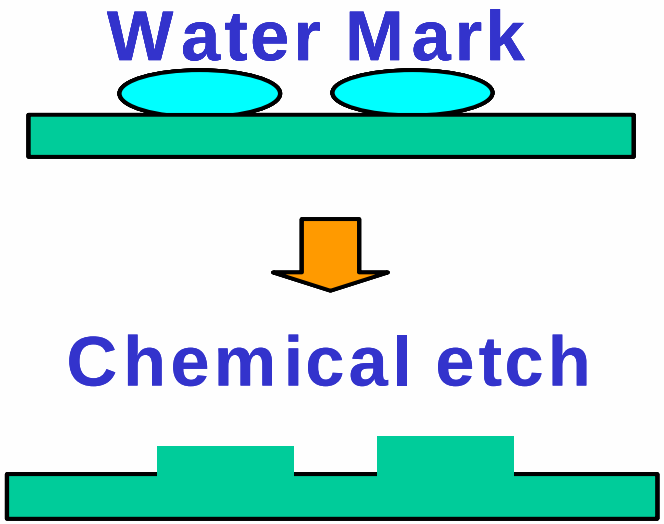
- **Background: Trimmer is used for wafer edge trimming before wafer bonding. The trimmer will induce many Si-dust particles in the trimming process.**
- **Trimmer Particle Reduction:**
  Optimizing clean recipe with brusher to remove the trimmer particle.

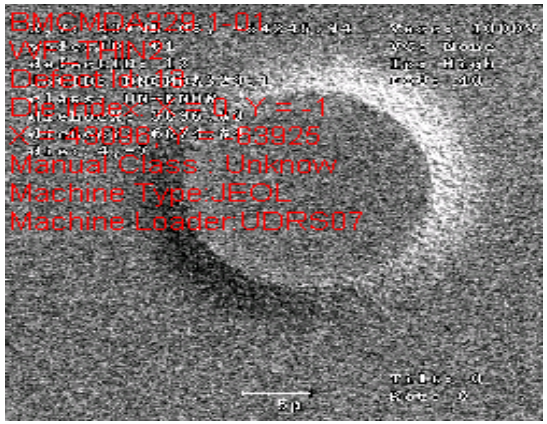




Surface Particle in Wet Thin Down

- After wet thin down high count coin defect shown in last wafer in each batch
- Coin Defect Reduction:
  - Containment Action: add dummy wafer after lot processing.
  - Long term Solution: :Window check for clean stage DIW time.

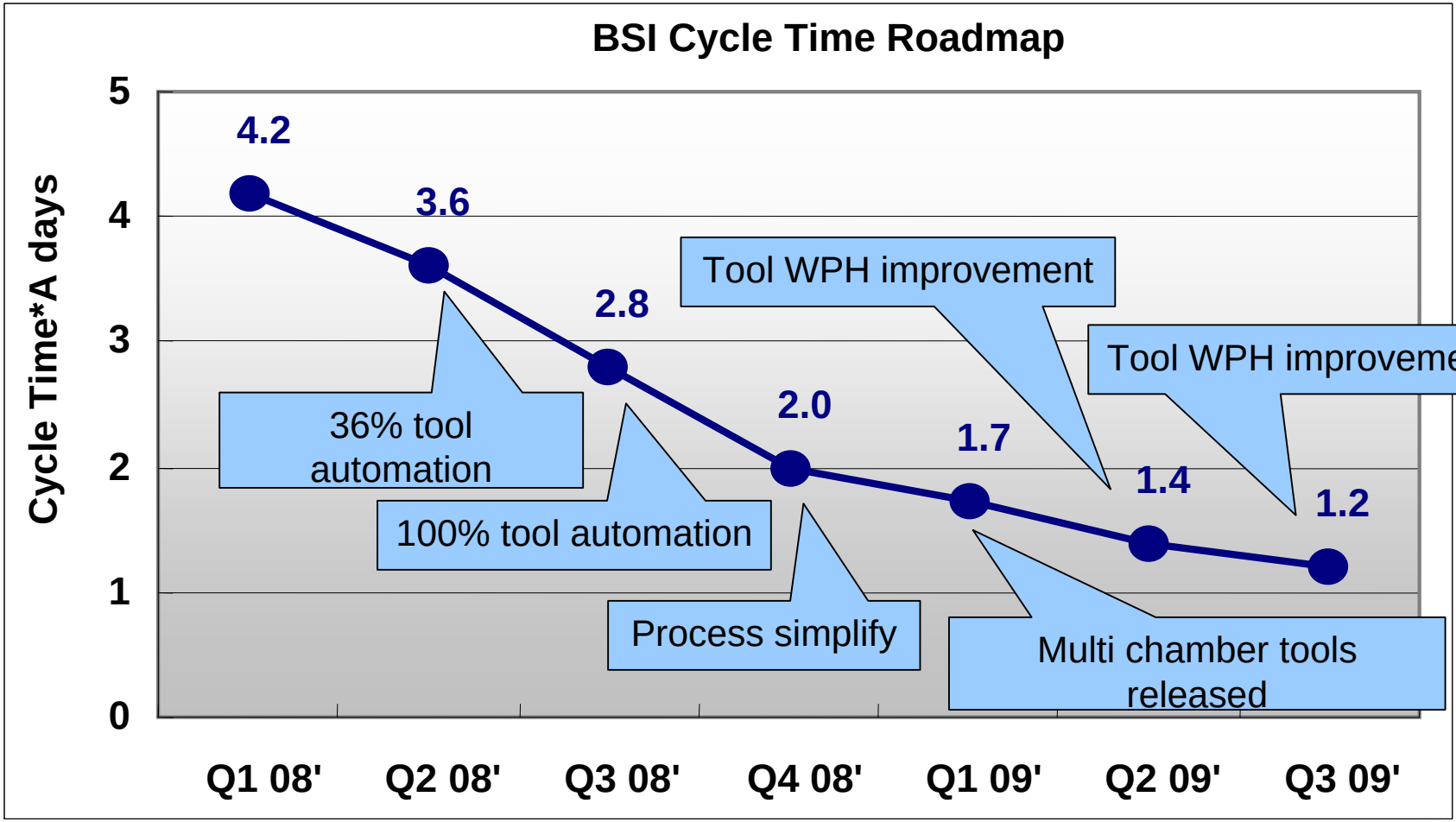




After Chemical etching coin defect shown in surface

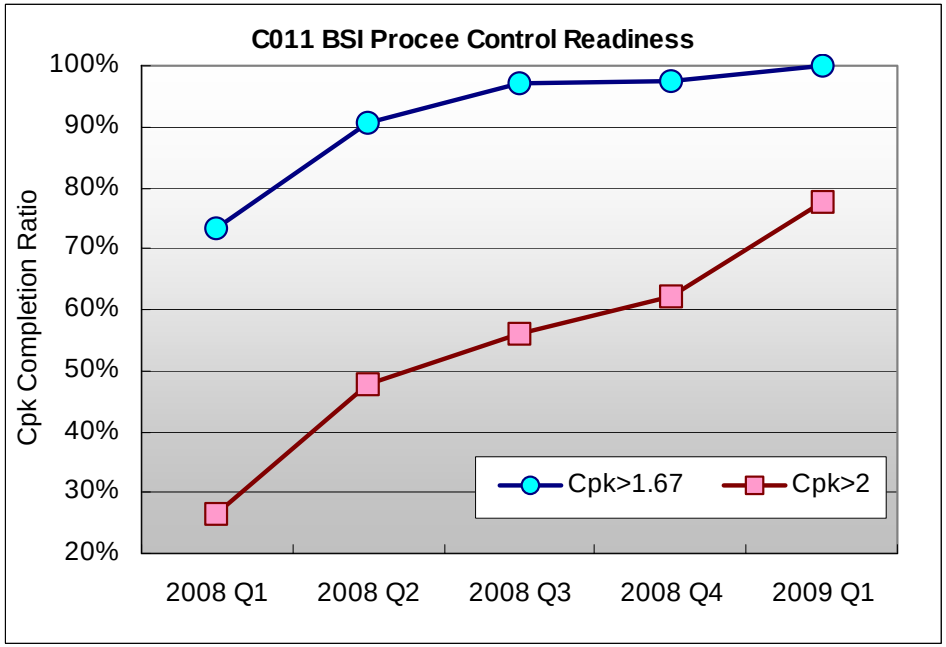
BSI Cycle-time Improvement

- 3.5A days cycle time reduction (4.2A → 1.2A)

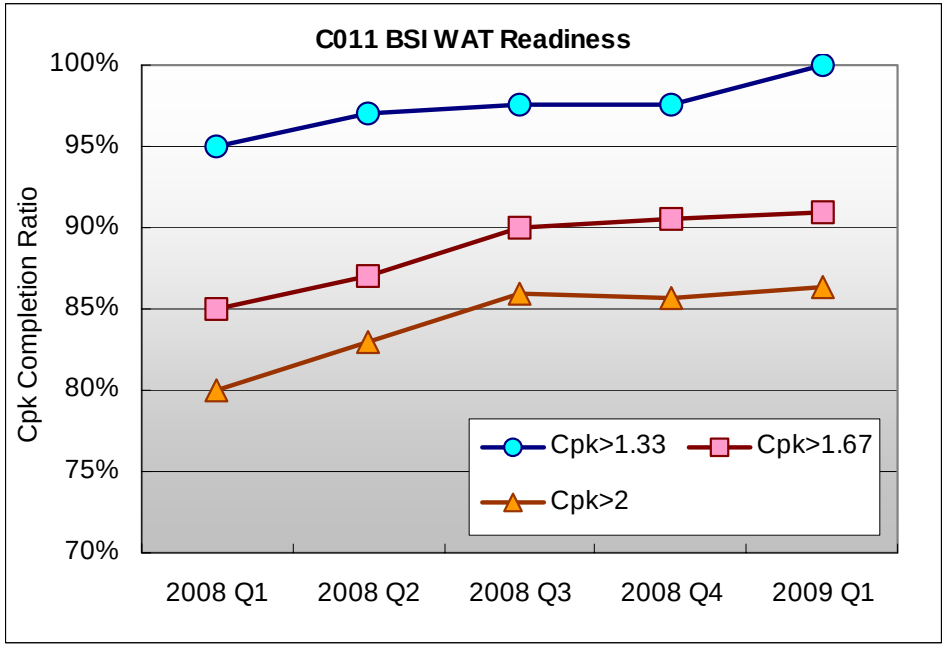


BSI SPC Control (In/Offline and WAT)

- **SPC control Cpk > 1.67 for in/offline monitor & Cpk> 1.33 for WAT by 2009 Q1**



BSI Process Control (In/Offline)



BSI WAT Index

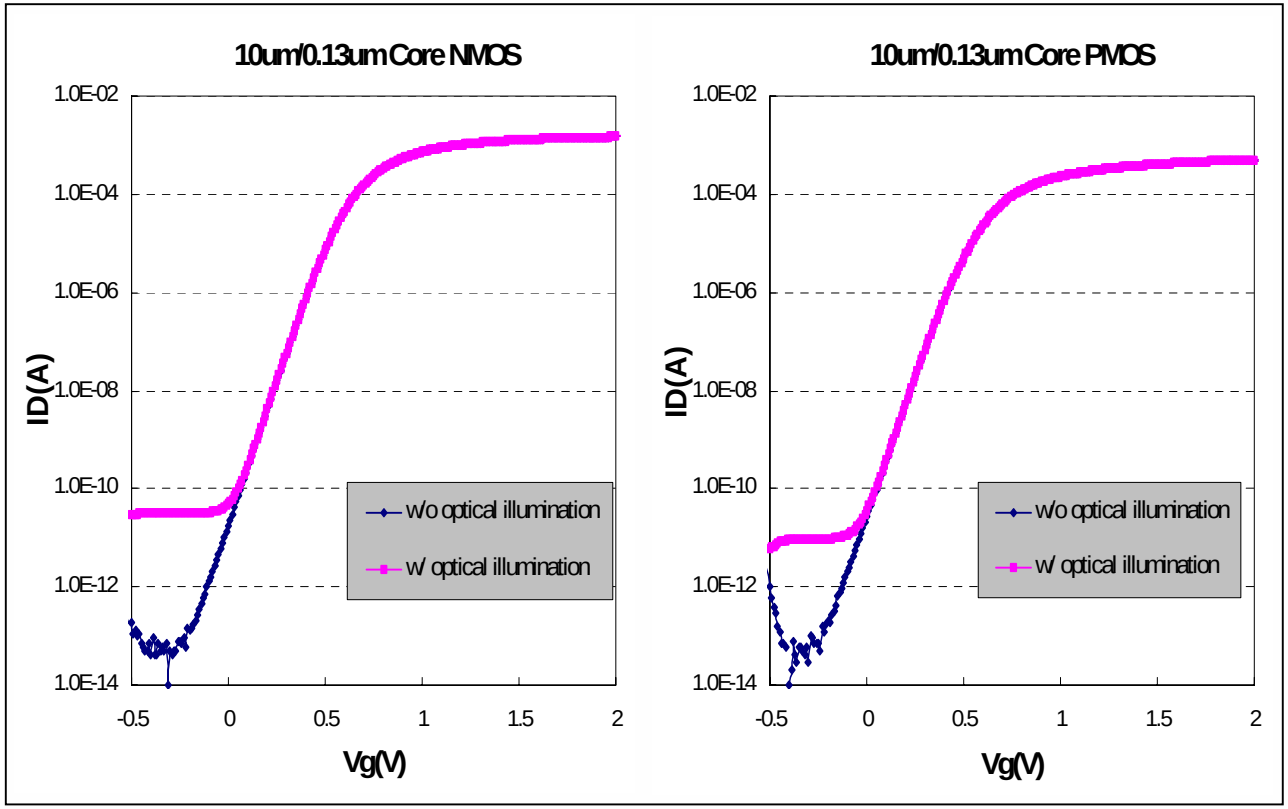
BSI Manufacturability

- Defect, particle, contamination are improved by optimizing chamber clean recipe and retrofitting tool hardware
- In line process monitor is performed by suitable Spec and metrology (FTIR, KLA, OP….)
- Cycle time is improved by high WPH(Wafer Per Hour) tool mixing run and automation run.
- Cost structure is improved by process/recipe simplification and low cost raw material
- SPC control Cpk> 1.67 for in/off line monitor & Cpk> 1.33 for WAT are achieved for BSI manufacturing

Device and Characterization

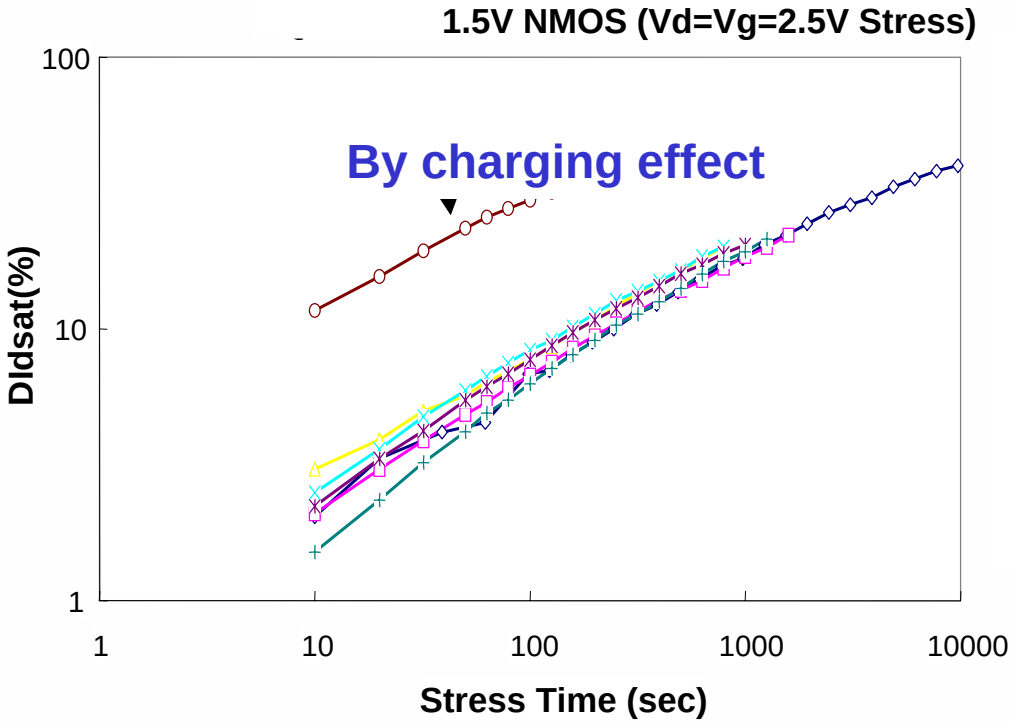
Device Performance

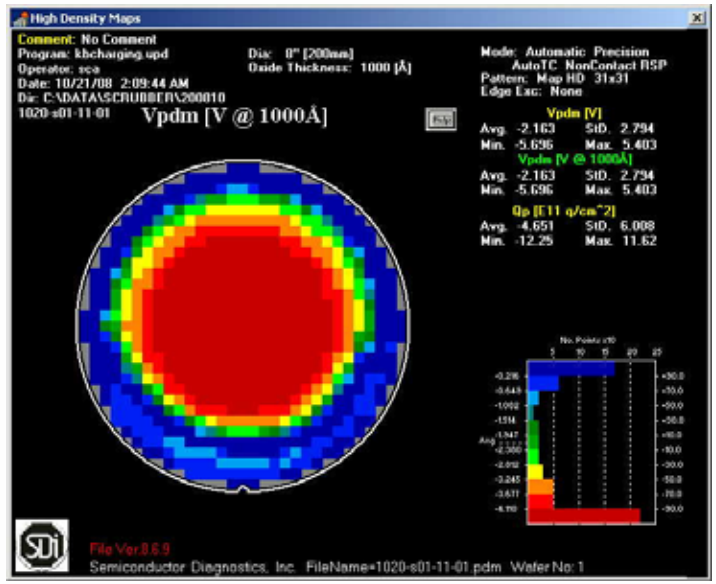
- MOS Id-Vds behavior w/i & w/o optical illumination
- Device at low current bias condition behaves differently under illumination due to photo carrier generation



Reliability with BSI Process

- N/PMOS w/ BSI process behaves the same performance as FSI after stress test.
- Device reliability associated with BSI thin-down process needs attention such as charging effect.
- N2H2 plasma treatment after laser anneal induces reliability failure

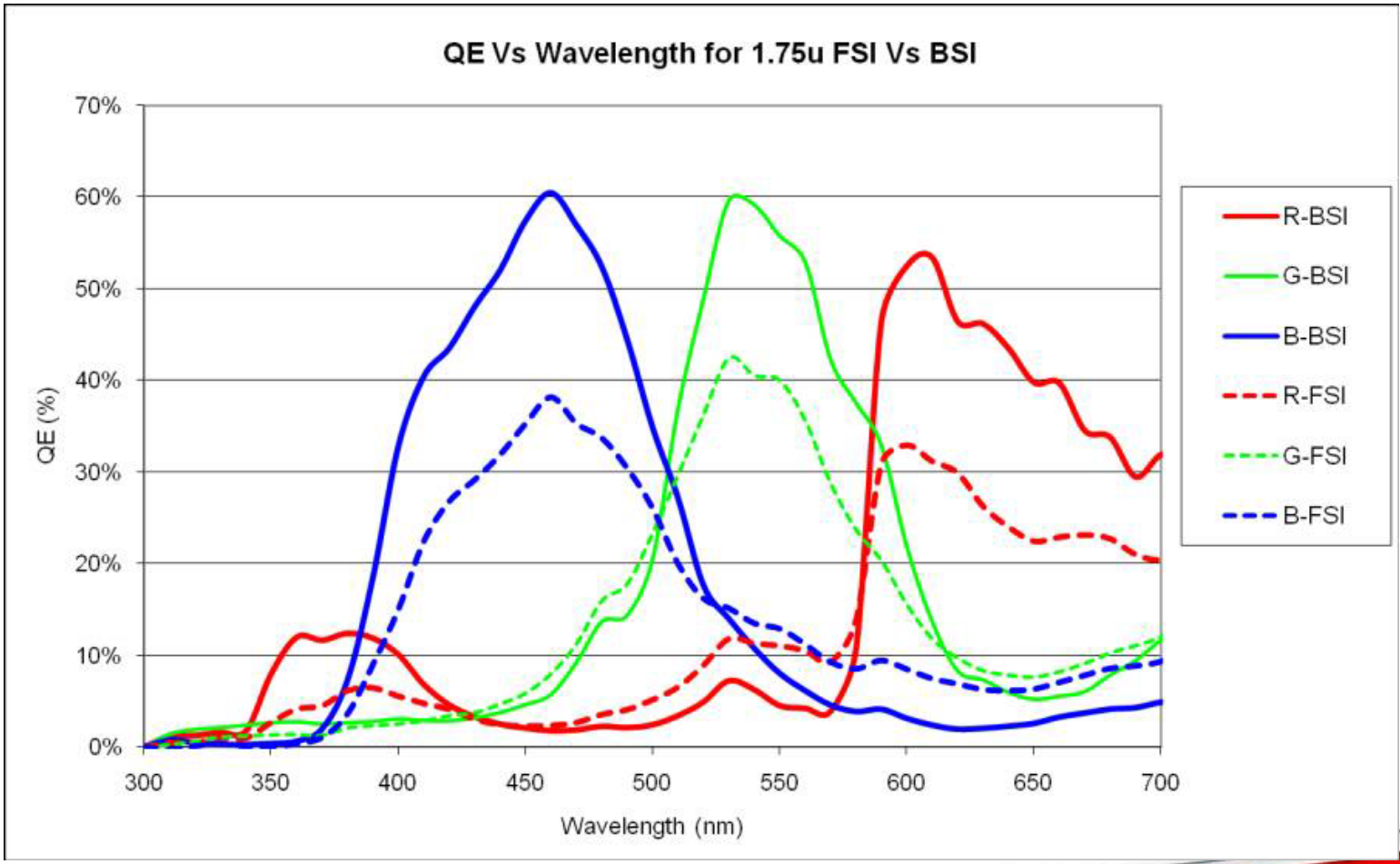




Wafer Map with Charging Test

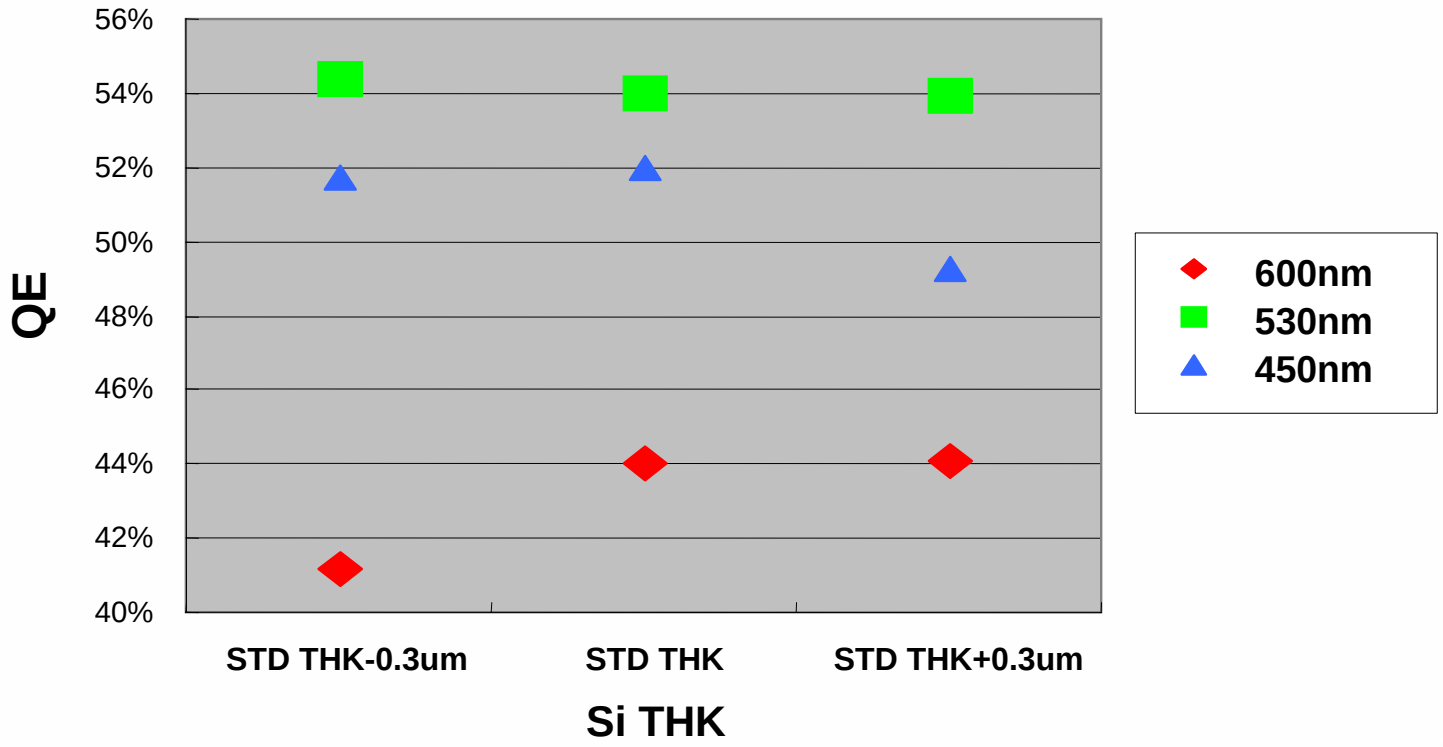
1.75um FSI vs BSI Performance

- **Quantum Efficiency: 40-60% improvement for BSI vs. FSI**
- **Crosstalk: 30-80% improvement for BSI vs. FSI**



QE versus Si THK

- On-target THK achieves optimized QE. Red and blue QE are more sensitive with THK control (~3% degradation with +-0.3um deviation)
- Thinner Si degrades red response and thicker Si degrades QE in blue (due to carrier recombination)

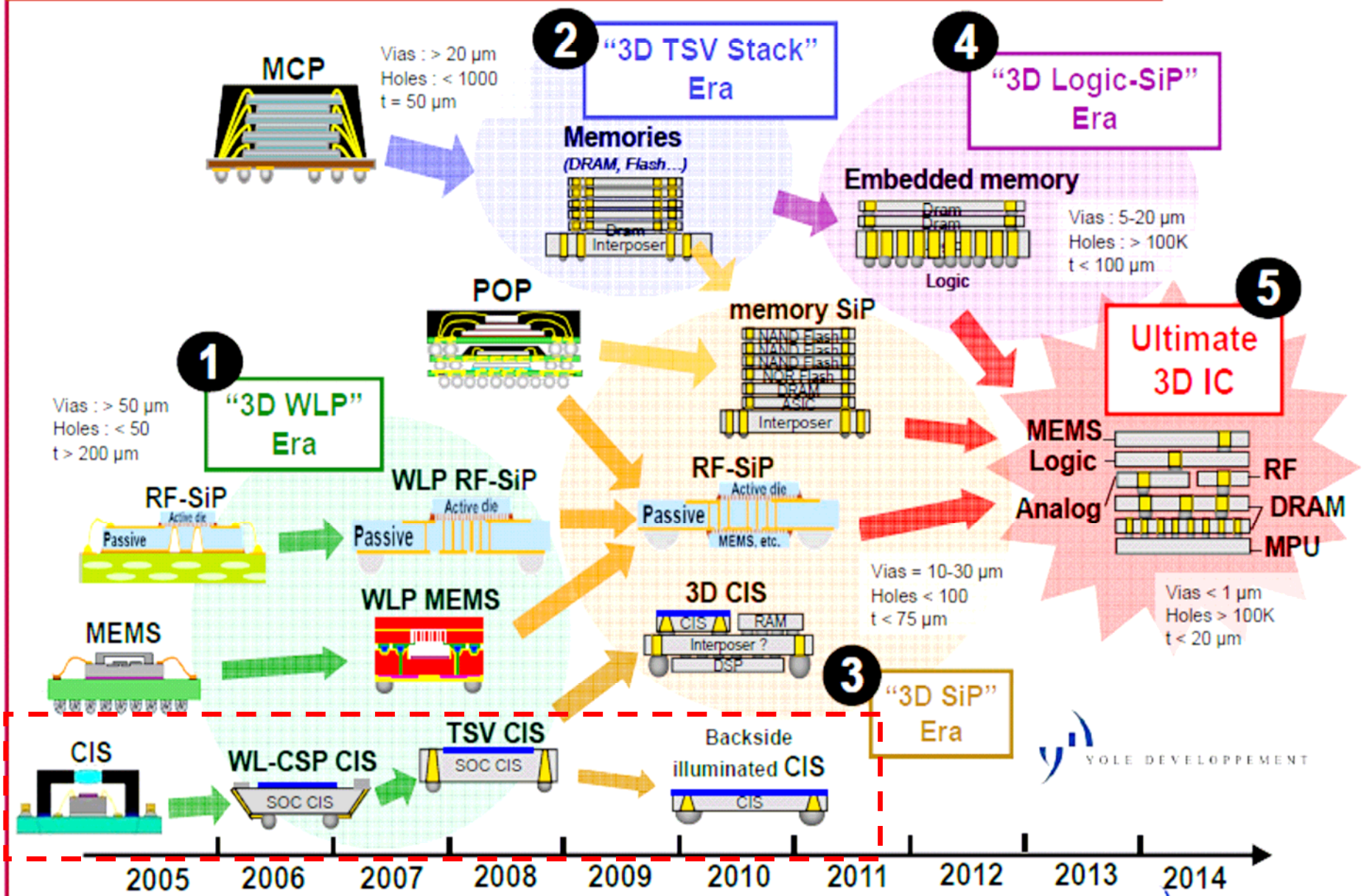


BSI Device Characterization Summary

- MOS transistors at low bias current condition behave differently due to optical illumination.
- Charging effect by BSI tools detected and improved for reliability
- Implementation of backside P+ imp with laser anneal and backside ARC significantly improves QE
- 1.75um FSI vs BSI comparison: 20%-30% improvement in QE (R/G/B); xtalk 28%-67% reduction
- Tight Si THK control is needed to avoid QE degradation (~3% QE deviation with +-0.3um Si control)

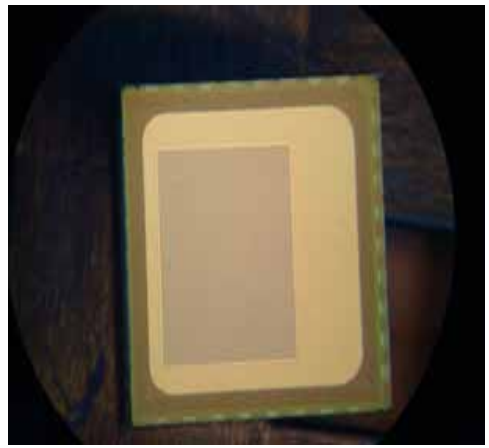
BSI Package Technology

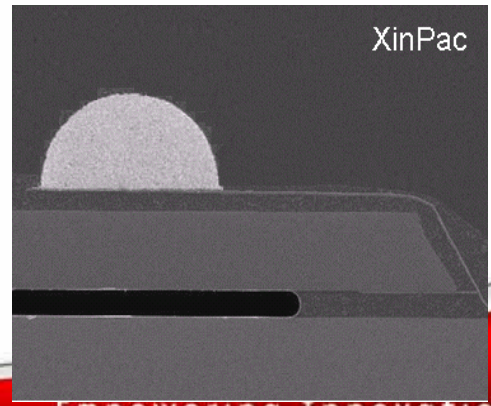
3D interconnect Technology Roadmap



Chip Scale Package(CSP) in BSI

- 1st Chip scale package on BSI in world wide
- Better Image sensitivity by cavity package
- Stress reduction in T-contact by XinPac-300(CSP3) technology
- XinPac-300 Key features
  - Min. scribe line width: 200um
  - Min. extension pad pitch: 300um
  - Total package high,exclude ball height : 605um





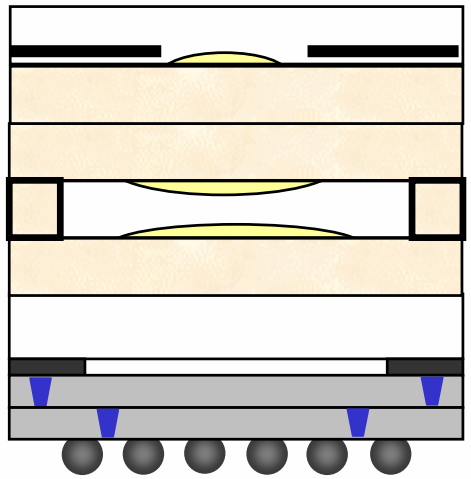
Advanced Camera Module Technology Integration Trend

BSI + TSV-CSP technology integration realize

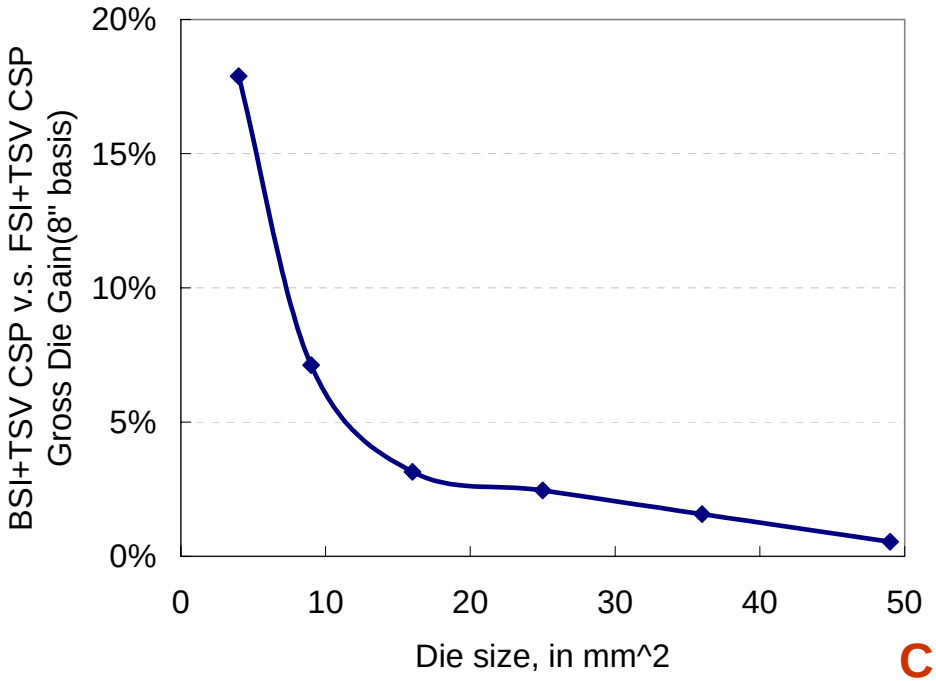
- **True chip size CSP solution**

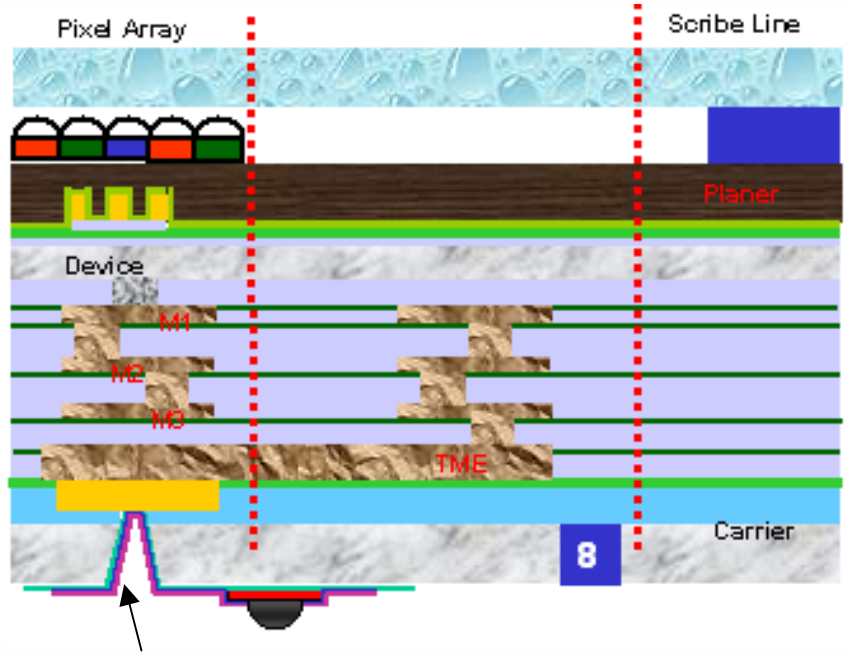
Compact camera module through integration with wafer level lens

Smart camera module by 3D CCM + DSP stacking



BSI + TSV CSP Benefits - More Gross Die





Circuit under pad

- **Circuit under pad design compatible and zero silicon real estate loss**
- **5%~15% gross die gain compare with conventional sidewall CSP**

BSI Package Technology Summary

- 0.11 BSI Achievements (BSI + CSP3) :
  - Achieve 1st Chip-Scale package on BSI in world wide
  - Good Stress reduction in T- Contact & Competitive stack height by CSP3 technology
- Next generation & future trend (BSI + TSV or 3D IC)
  - Smaller die size compare with COB/CSP3 solution
  - More gross dies through CUP compatible design
  - Enable low cost CCM (Compact Camera Module) via integration with wafer level lens module technology
  - Enhanced CSP reliability compared with conventional sidewall CSP technology
  - Enable pixel level interconnection through TSV technology

Summary & Future Trend

Summary

- World's first BSI image sensor w/ bulk Si in mass production – 1.75um & 1.4um pixel
- Utilization of epi wafers for BSI mass production with well Si THK control
- Achieve more than 5x QE enhancement in BSI by backside P+ implant and ARC coating
- Achieve dark current < 1 e/sec @ RT by surface optimization
- Achieve record low SNR=10 lux value -- 57 lux for 1.75um pixel and 105 lux for 1.4um pixel
- N65 BSI for 1.1 um pixel and beyond is under development and demonstrates the convincing manufacturing capability in 12" Cu Fab

5 Mega 1.4um Pixel Performance

Dark current < 1 e/sec , QE >50%; Excellent Color cross talk

BSI Future Work

- Tighter Epi-Si thickness control (< ±0.5um → < ±0.1um) on in-coming materials in order to further improve within wafer thickness uniformity (< ±0.1um)
- Laser hardware improvement to tighten energy uniformity for Rs uniformity improvement (< 1.5%)
- Yield enhancement through tight thickness control, uniform backside P+ activation, defect reduction & robust wafer edge engineering
- Process cost down; WPH (Wafer Per Hour) improvement & Process simplification, etc.
- CFA optimization to target 1.1um/0.9um pixel sizes and beyond in 300mm manufacturing.
- TSV + CSP integration with BSI and wafer level camera module.

Reference

- Tom Joy et al, “Development of a production-ready, back-illuminated CMOS image sensor with small pixels”, IEDM, p1007, 2007.
- Bedabrata Pain et al, “Wafer-level thinned CMOS imagers implemented in a bulk-CMOS technology”, IISW, 2007.
- Jens Primd et al, “A 3mega-pixel back-illuminated image sensor in 1T5 architecture with 1.45um pixel pitch”, IISW, 2007.
- Shin Iwabuchi et al, “A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring”, ISSCC, p302, 2006.
- Jung Chak Ahn et al, “Advanced image sensor technology for pixel scaling down toward 1.0um (Invited)”, IEDM, p275, 2008.